

Model Name: GA-Z87X-OC

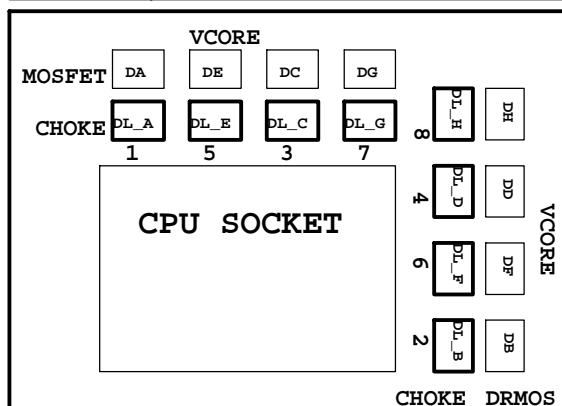
Rev 1.03

SHEET TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1155-A
05	CPU_LGA1155-B
06	CPU_LGA1155-C
07	DDR III CHANNEL A
08	DDR III CHANNEL B
09	PCH_FDI,DMI,USB,PCIE,NVRAM
10	PCH_DP,CLK BUFFER
11	PCH_HOST,SATA,PCI
12	PCH_GPIO,CTRL,AUDIO
13	PCH_PWR,GND
14	PCH HDMI/DP
15	PCI EXPRESS*16 SLOT
16	PCI EXPRESS*8 SLOT
17	PCI EXPRESS*1 SLOTS X1
18	PCI EXPRESS X8 X4 SWITCH
19	PCI EXPRESS*4 SLOT (CPU)
20	PCI EXPRESS*4 SLOT (PCH)
21	ITE 8892
22	PCI SLOT 1&2
23	ALC892
24	REAR AUDIO JACK
25	Dual BIOS
26	IR3563A PWM
27	IR3550-VCORE

SHEET TITLE

28	IR3570-DDR PWM
29	IR3598-DDR POWER
30	5VDUAL, 3VDAUL, ERP
31	PCH1.05V, PCH1.5V, VCC3_DAC
32	I/O ITE8728
33	KB/USB3
34	F_PANEL , F_USB , PHOT
35	F_USB 2.0
36	F_USB 3.0
37	ATX POWER, CLOCK GEN
38	HWM, FAN CTRL
39	INTEL I217
40	Highly switch
41	RST, PWR, CLR_CMOS
42	IT 8790
43	FAN CTRL
44-45	RENESAS USB3.0 HUB_A
46-48	RENESAS USB3.0 HUB_B
49	TABLE LIST



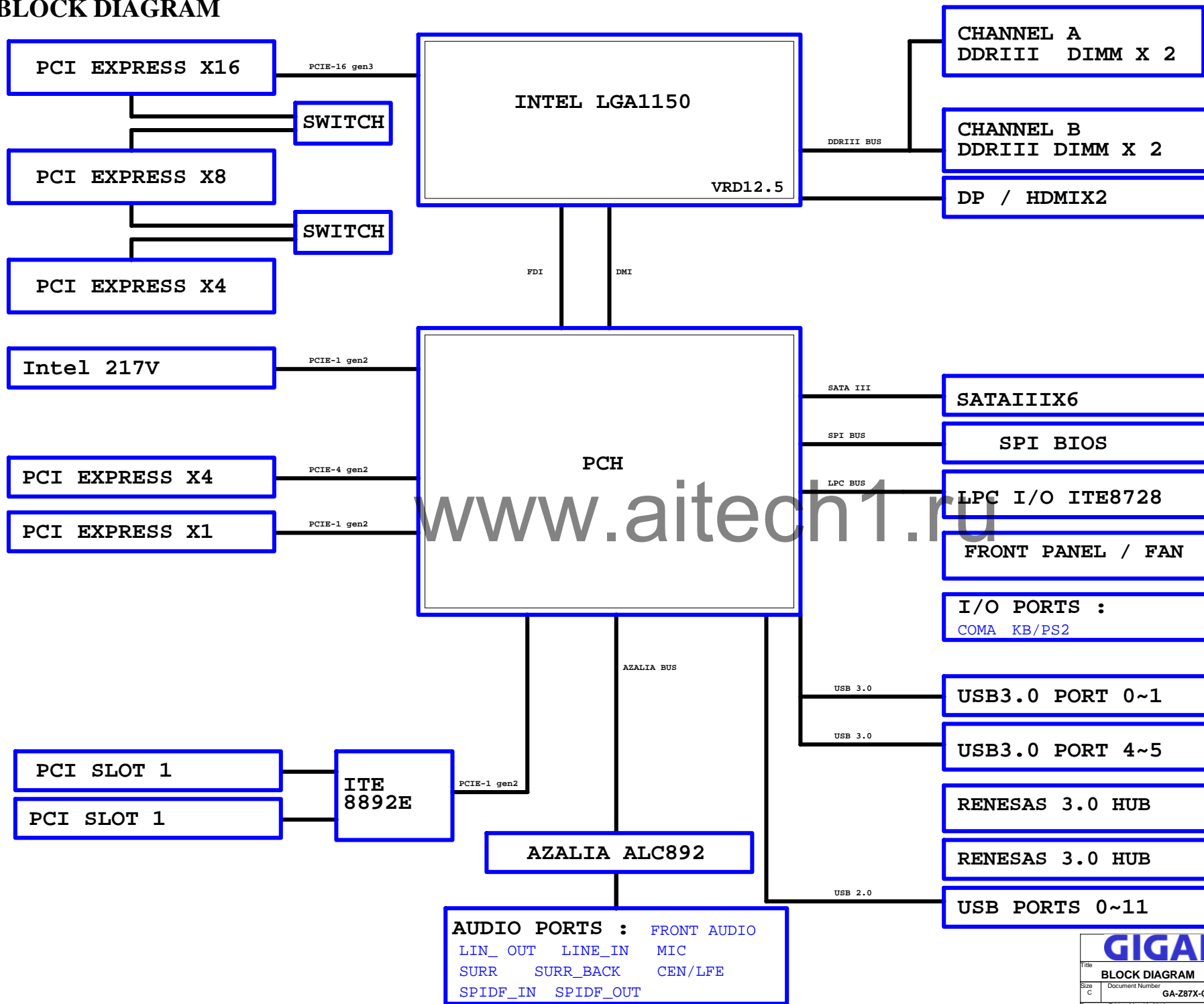
GIGABYTE™		
Title Cover Sheet		
Size Custom	Document Number GA-Z87X-OC	Rev 1.03
Date: Friday, May 10, 2013 Sheet 1 of 49		

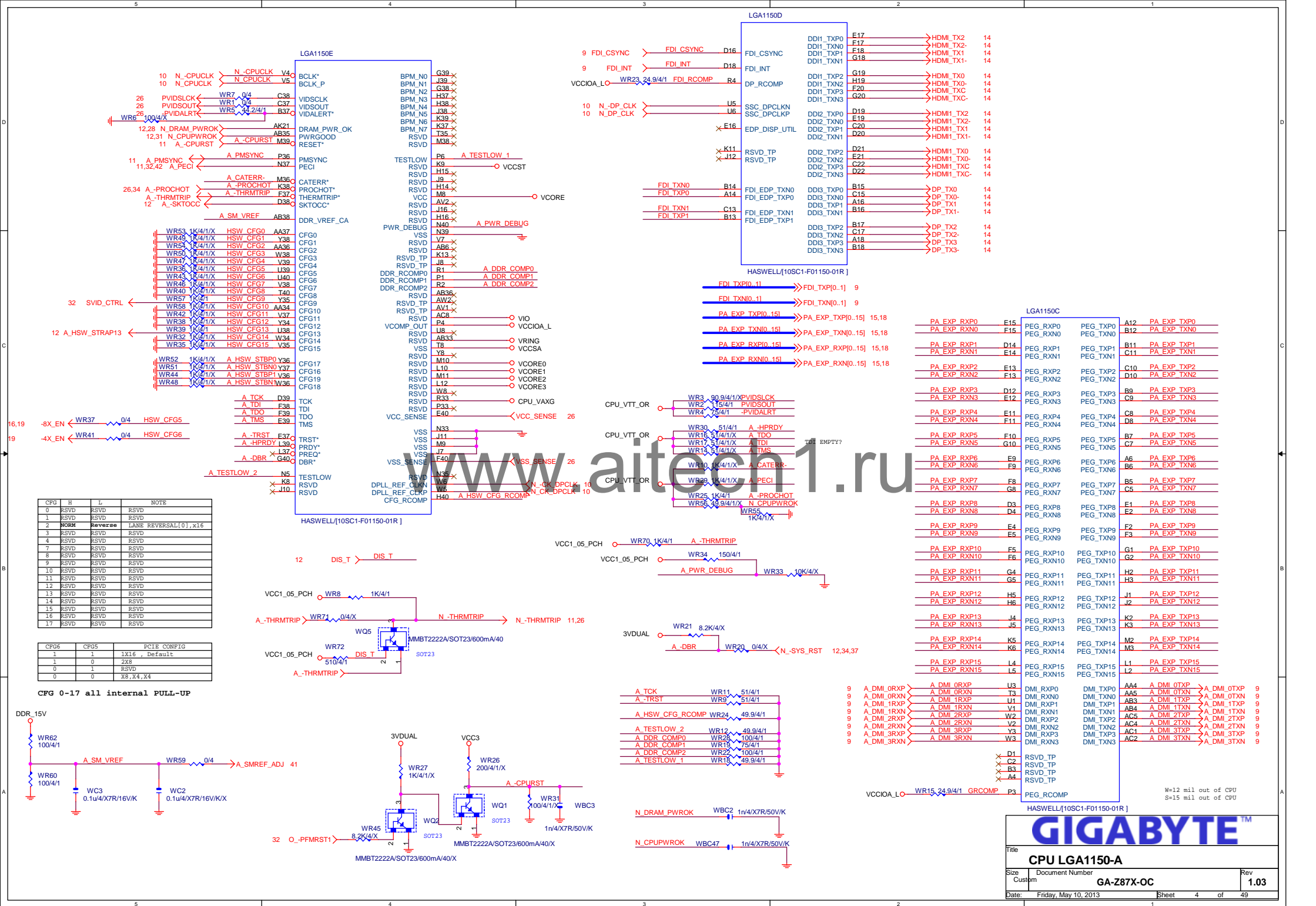
Component value change history

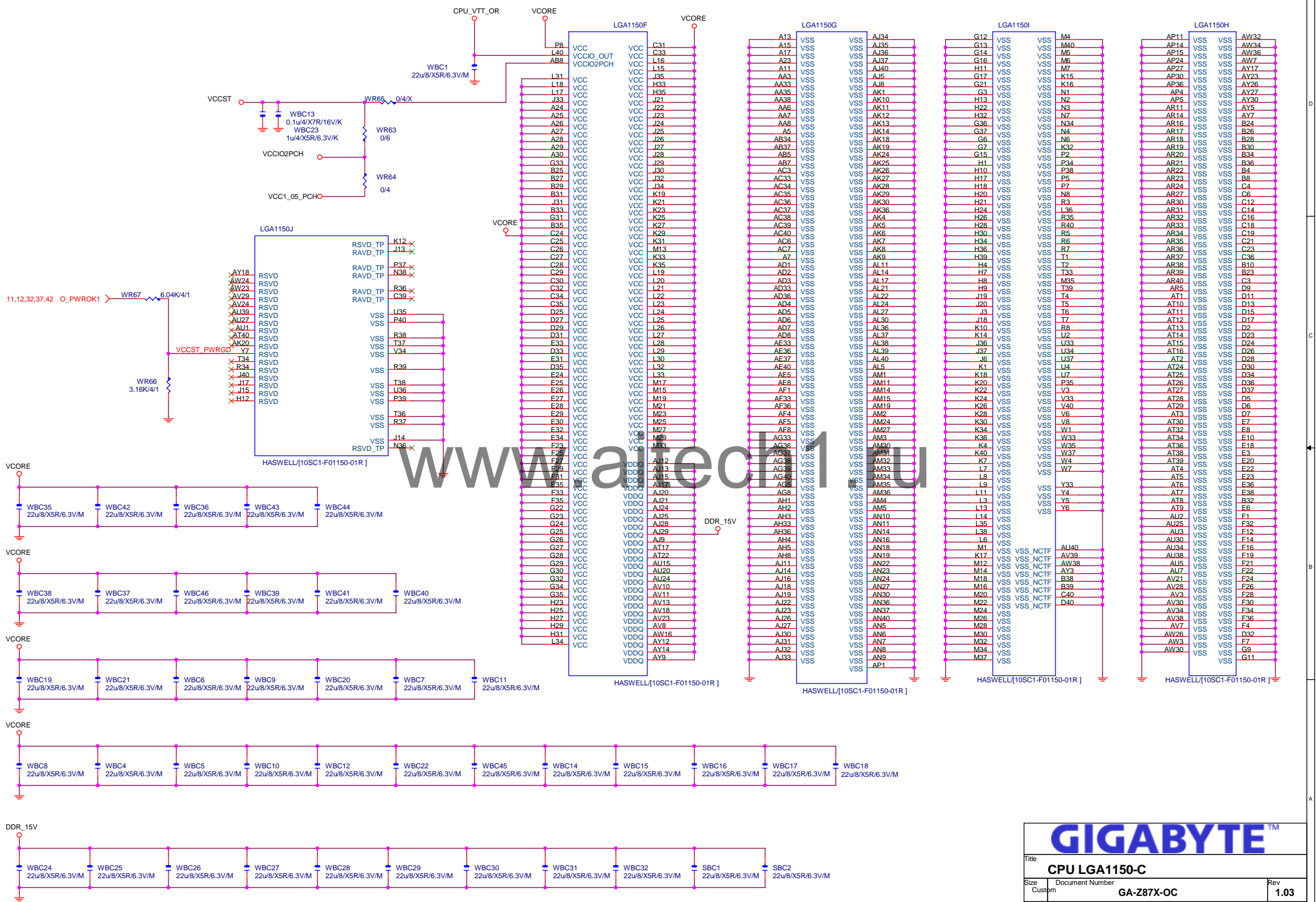
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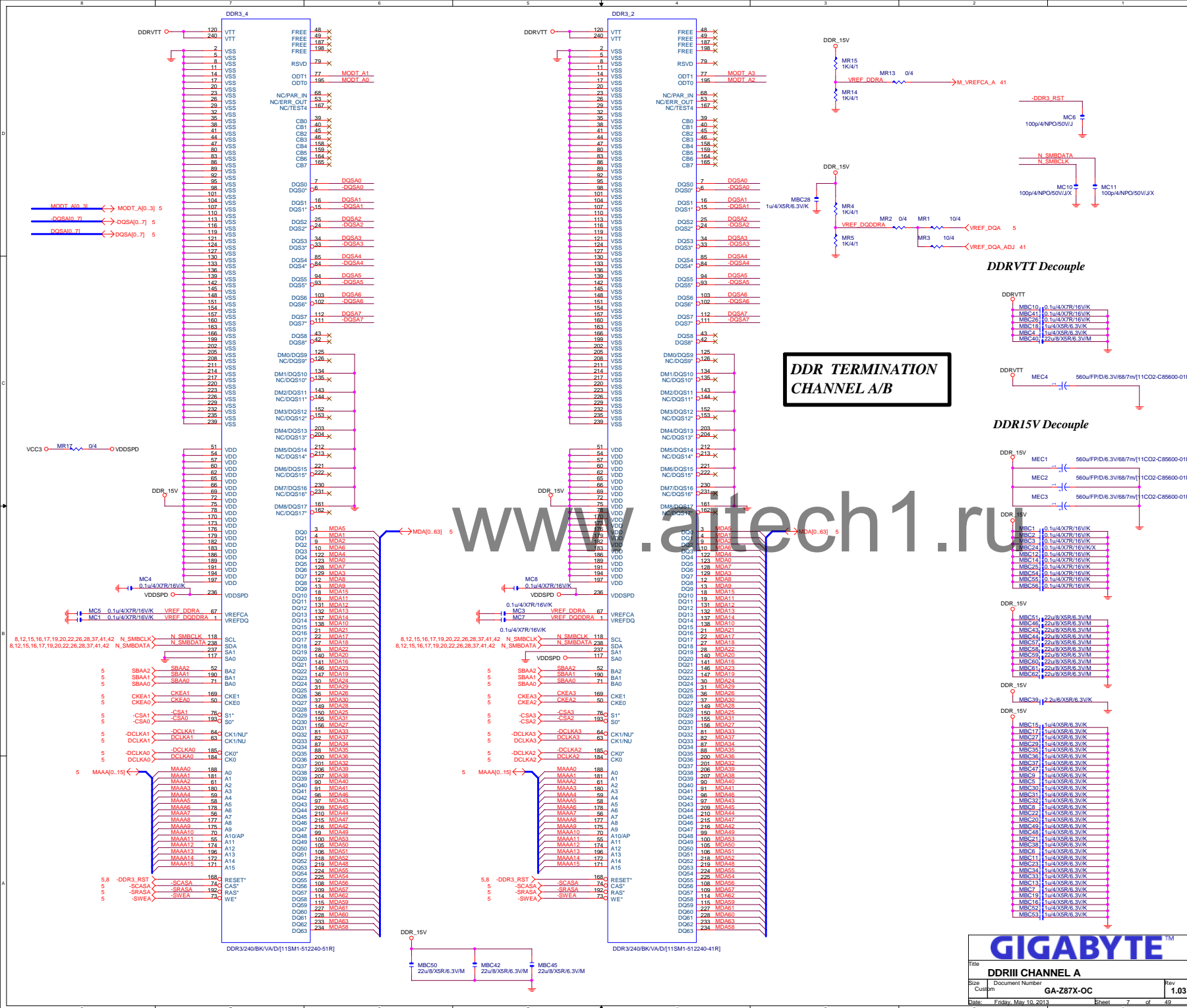
DATE	Change Item	Reason
2012/12/21	REV0.1 Z87X-OC 0.1 gerber out	
2013/02/18	0.2B modify SATA 線路	
2013/03/08	1.0B modify 8790 線路 1.0B modify FAN 線路	
2013/03/29	1.01B modify HUB 線路 1.01B modify PCIE_SW 線路 1.01B modify OTP 線路	
2012/04/12	1.02B modify 文字面	
2013/04/16	1.03B modify OC_IGNITION 線路	

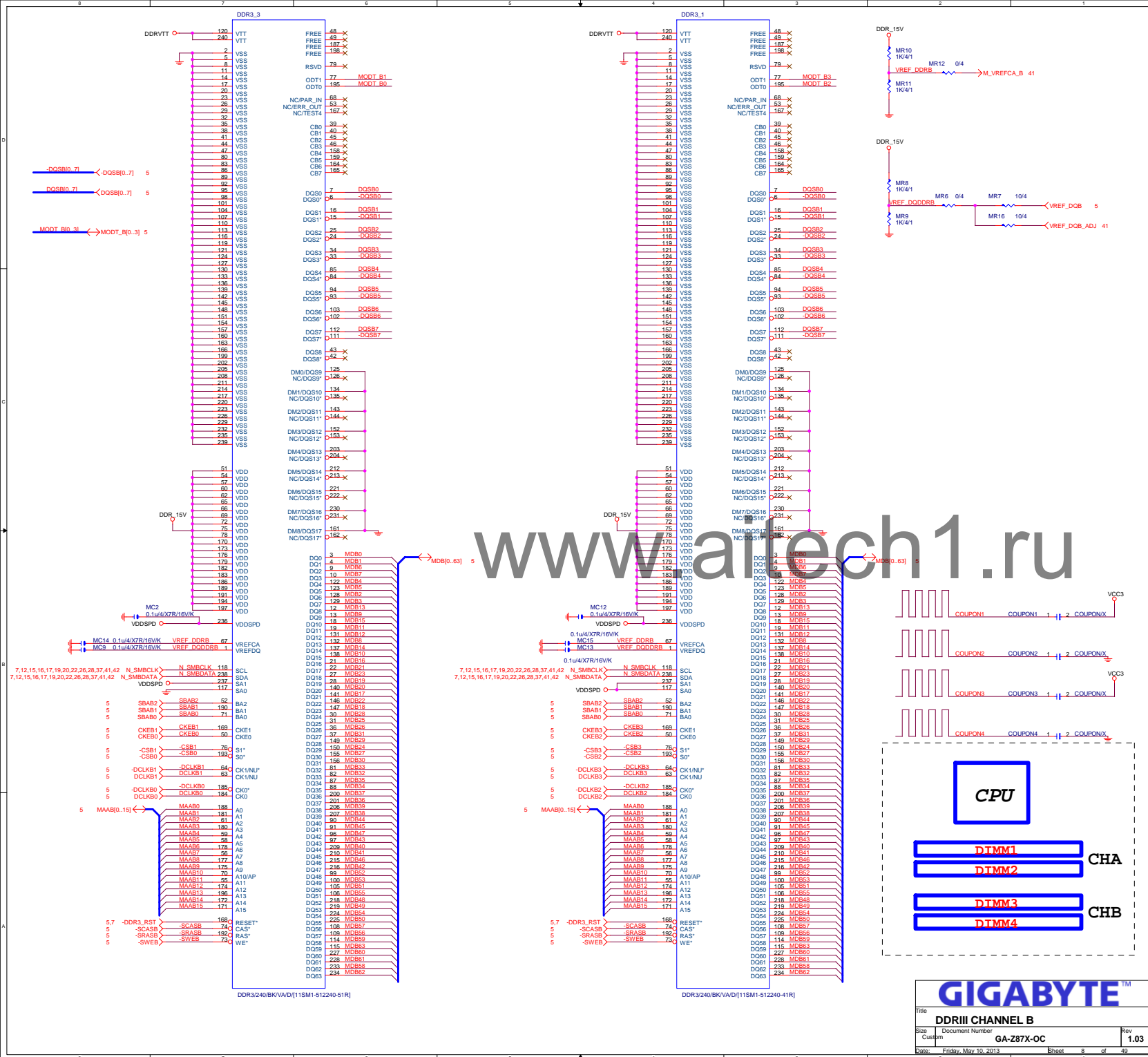
BLOCK DIAGRAM

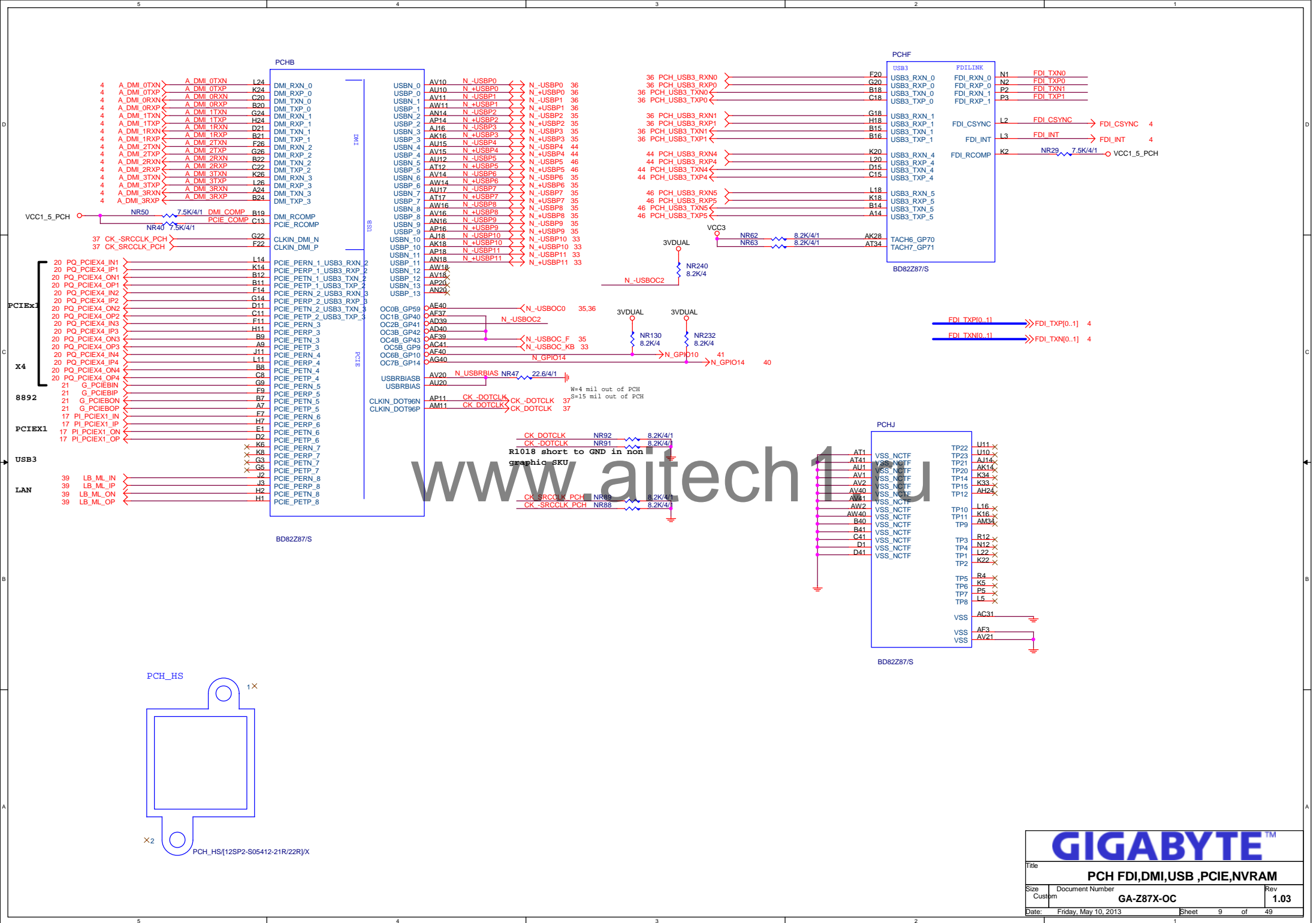


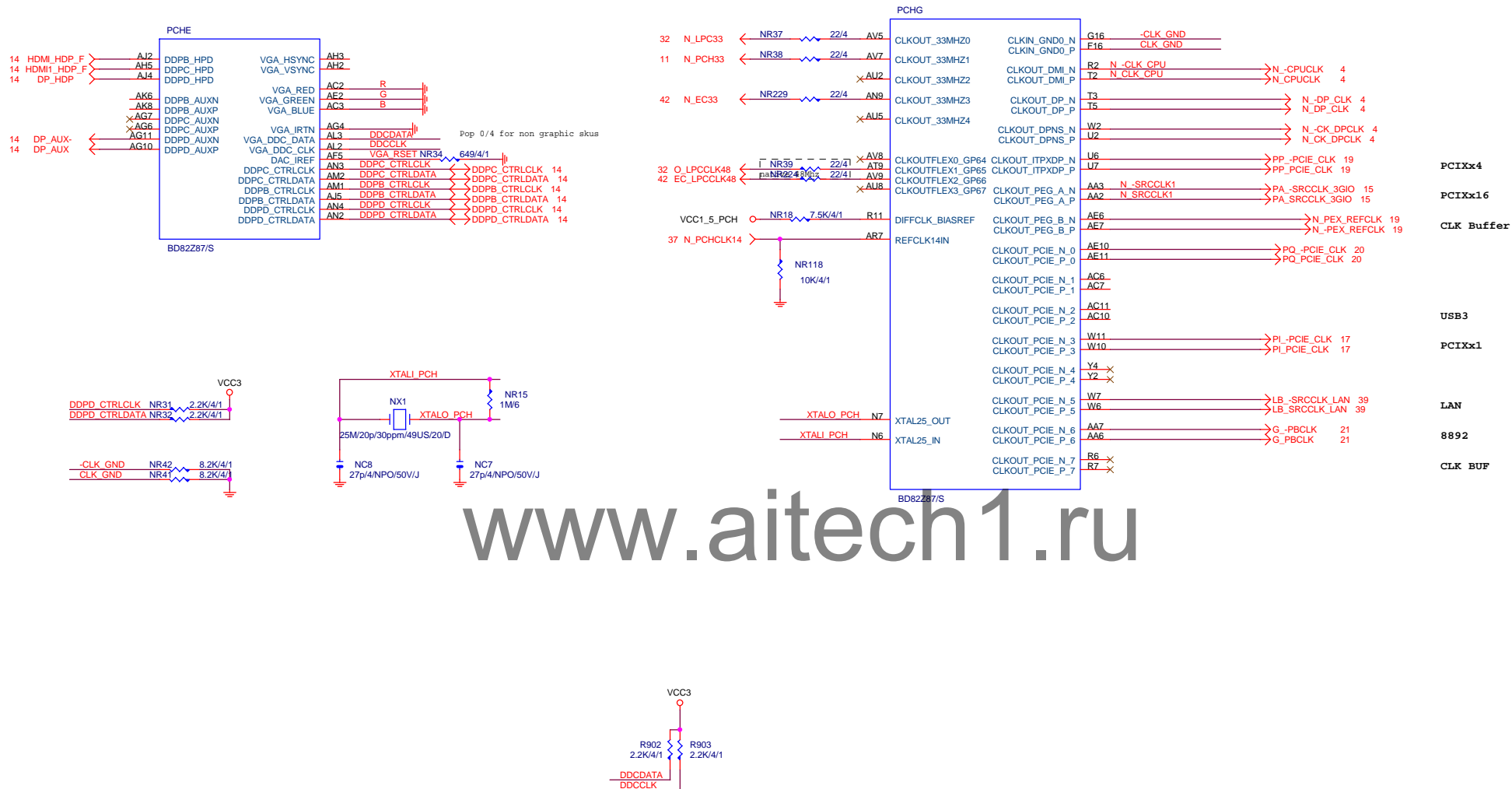




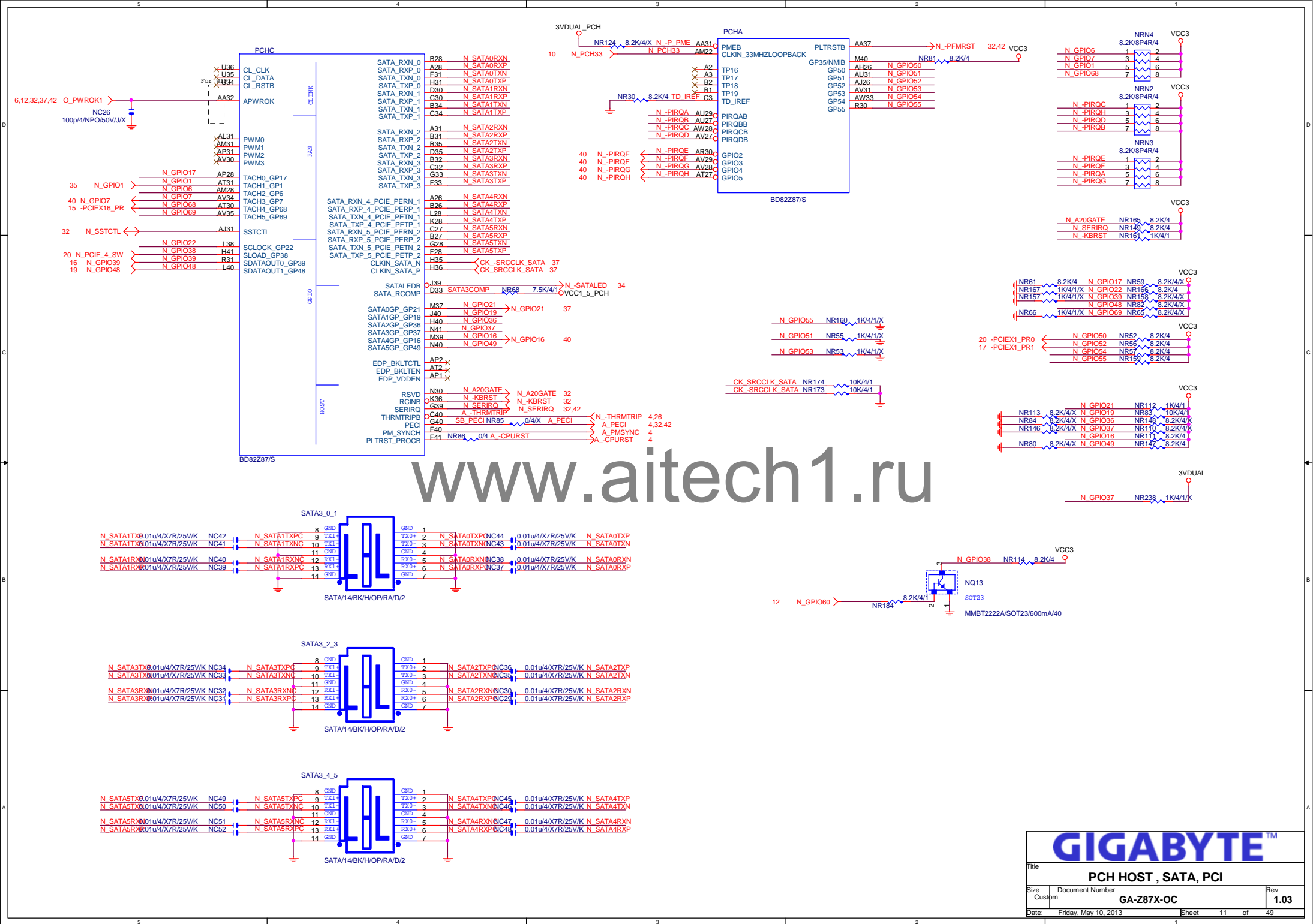




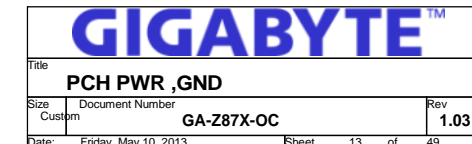


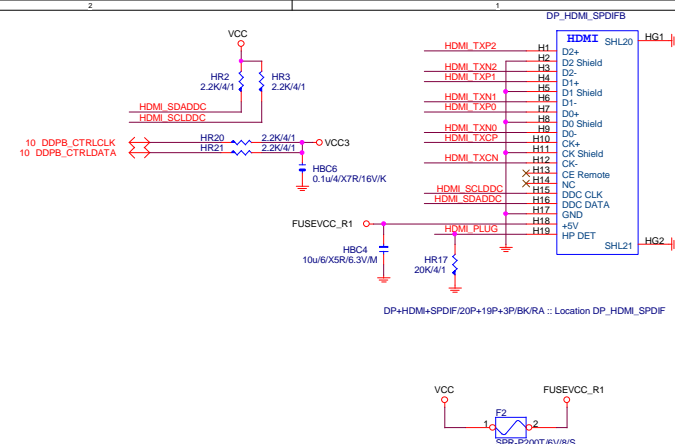


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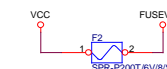




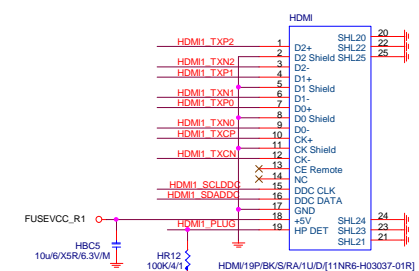
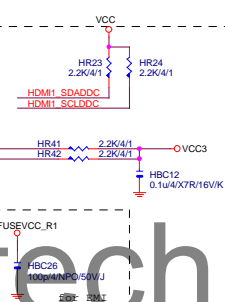




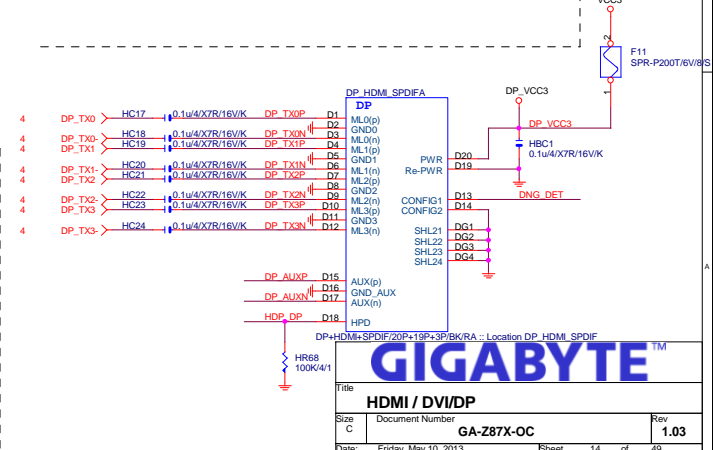
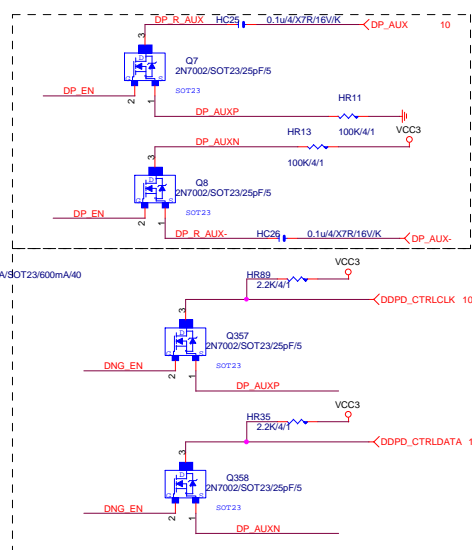
DP+HDMI+SPDIF/20P+19P+3P/BK/RA :: Location DP_HDMI_SPDIF



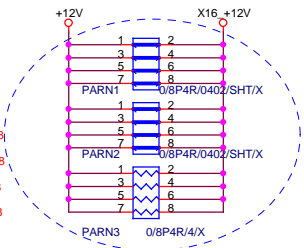
0 1:7.2dB



— — — — —



**+12 protect
short-wire test**



PCIE16:16/5/5/16

PA_EXP_RXP0_15I >> PA_EXP_RXP0[0..15] 4,18
PA_EXP_RXN0_15I >> PA_EXP_RXN0[0..15] 4,18
PA_EXP_TXP0_15I >> PA_EXP_TXP0[0..15] 4,18
PA_EXP_TXN0_15I >> PA_EXP_TXN0[0..15] 4,18

PA_EXP_TXP0	PAC5	0.22u/4/X5R/6.3V/K	PA_EXP_TXP0_C
PA_EXP_TXN0	PAC4	0.22u/4/X5R/6.3V/K	PA_EXP_TXN0_C
PA_EXP_TXP1	PAC6	0.22u/4/X5R/6.3V/K	PA_EXP_TXP1_C
PA_EXP_TXN1	PAC7	0.22u/4/X5R/6.3V/K	PA_EXP_TXN1_C
PA_EXP_TXP2	PAC8	0.22u/4/X5R/6.3V/K	PA_EXP_TXP2_C
PA_EXP_TXN2	PAC9	0.22u/4/X5R/6.3V/K	PA_EXP_TXN2_C
PA_EXP_TXP3	PAC10	0.22u/4/X5R/6.3V/K	PA_EXP_TXP3_C
PA_EXP_TXN3	PAC11	0.22u/4/X5R/6.3V/K	PA_EXP_TXN3_C
PA_EXP_TXP4	PAC12	0.22u/4/X5R/6.3V/K	PA_EXP_TXP4_C
PA_EXP_TXN4	PAC13	0.22u/4/X5R/6.3V/K	PA_EXP_TXN4_C
PA_EXP_TXP5	PAC14	0.22u/4/X5R/6.3V/K	PA_EXP_TXP5_C
PA_EXP_TXN5	PAC15	0.22u/4/X5R/6.3V/K	PA_EXP_TXN5_C
PA_EXP_TXP6	PAC16	0.22u/4/X5R/6.3V/K	PA_EXP_TXP6_C
PA_EXP_TXN6	PAC17	0.22u/4/X5R/6.3V/K	PA_EXP_TXN6_C
PA_EXP_TXP7	PAC18	0.22u/4/X5R/6.3V/K	PA_EXP_TXP7_C
PA_EXP_TXN7	PAC19	0.22u/4/X5R/6.3V/K	PA_EXP_TXN7_C
PA_EXP_SW_TXP8	PAC21	0.22u/4/X5R/6.3V/K	PA_EXP_SW_TXP8_C
PA_EXP_SW_TXN8	PAC20	0.22u/4/X5R/6.3V/K	PA_EXP_SW_TXN8_C
PA_EXP_SW_TXP9	PAC22	0.22u/4/X5R/6.3V/K	PA_EXP_SW_TXP9_C
PA_EXP_SW_TXN9	PAC23	0.22u/4/X5R/6.3V/K	PA_EXP_SW_TXN9_C
PA_EXP_SW_TXP10	PAC24	0.22u/4/X5R/6.3V/K	PA_EXP_SW_TXP10_C
PA_EXP_SW_TXN10	PAC25	0.22u/4/X5R/6.3V/K	PA_EXP_SW_TXN10_C
PA_EXP_SW_TXP11	PAC26	0.22u/4/X5R/6.3V/K	PA_EXP_SW_TXP11_C
PA_EXP_SW_TXN11	PAC27	0.22u/4/X5R/6.3V/K	PA_EXP_SW_TXN11_C
PA_EXP_SW_TXP12	PAC28	0.22u/4/X5R/6.3V/K	PA_EXP_SW_TXP12_C
PA_EXP_SW_TXN12	PAC29	0.22u/4/X5R/6.3V/K	PA_EXP_SW_TXN12_C
PA_EXP_SW_TXP13	PAC30	0.22u/4/X5R/6.3V/K	PA_EXP_SW_TXP13_C
PA_EXP_SW_TXN13	PAC31	0.22u/4/X5R/6.3V/K	PA_EXP_SW_TXN13_C
PA_EXP_SW_TXP14	PAC32	0.22u/4/X5R/6.3V/K	PA_EXP_SW_TXP14_C
PA_EXP_SW_TXN14	PAC33	0.22u/4/X5R/6.3V/K	PA_EXP_SW_TXN14_C
PA_EXP_SW_TXP15	PAC34	0.22u/4/X5R/6.3V/K	PA_EXP_SW_TXP15_C
PA_EXP_SW_TXN15	PAC35	0.22u/4/X5R/6.3V/K	PA_EXP_SW_TXN15_C

PA_EXP_SW_RXP8_15I >> PA_EXP_SW_RXP8[8..15] 18
PA_EXP_SW_RXN8_15I >> PA_EXP_SW_RXN8[8..15] 18
PA_EXP_SW_TXP8_15I >> PA_EXP_SW_TXP8[8..15] 18
PA_EXP_SW_TXN8_15I >> PA_EXP_SW_TXN8[8..15] 18

PCI-E REV:1.1--> 2.5GHZ

PCE-E X1(單向) BANDWIDTH=2.5GHz*(8b/10b)=2Gb/s=250MB/s

PCE-E X1(雙向) BANDWIDTH=2.5GHz*(8b/10b)X2=4Gb/s=500MB/s

PCE-E X16(單向) BANDWIDTH=2.5GHz*(8b/10b)X16=32Gb/s=4GB/s

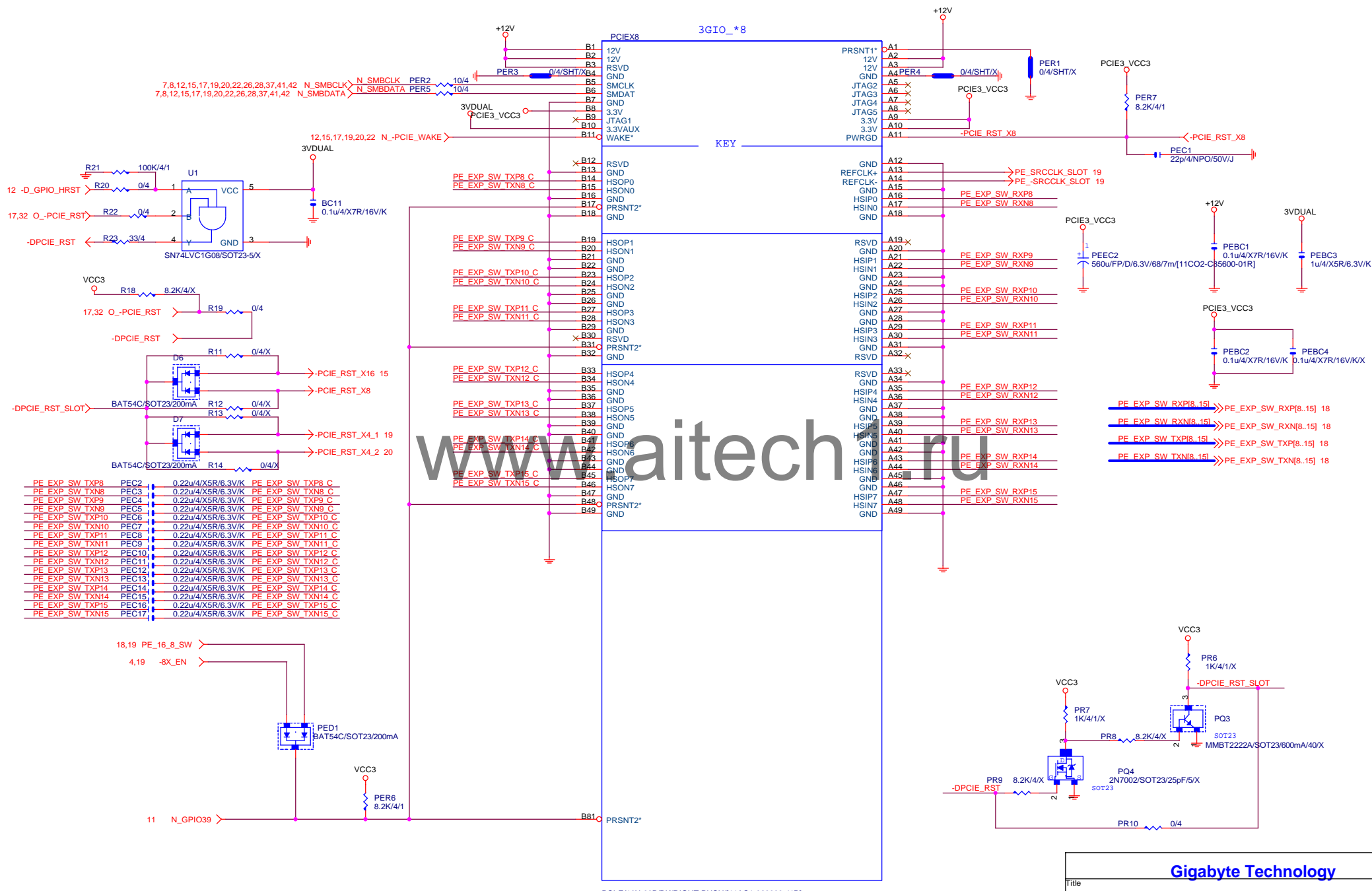
PCE-E X16(雙向) BANDWIDTH=2.5GHz*(8b/10b)X16X2=64Gb/s=8GB/s

PCI-E REV:2.0--> 5GHZ

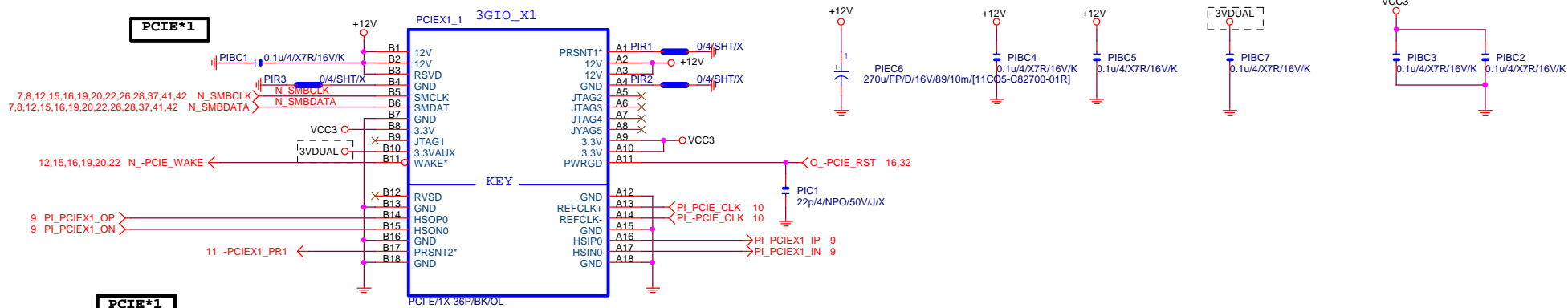
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PCI-E/16X-164P/BK/RIGHT PUSH/[11AC1-023164-81R]

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Title PCI EXPRESS * 16		
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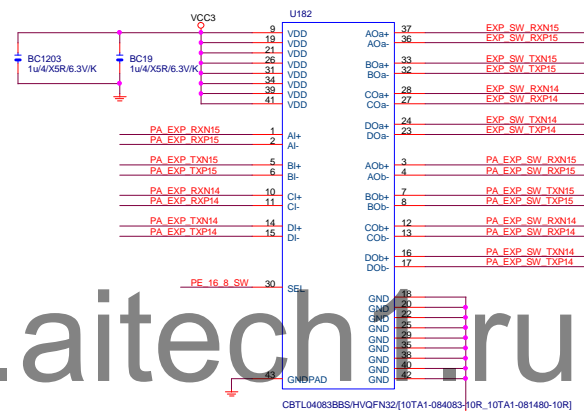
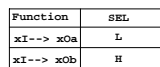


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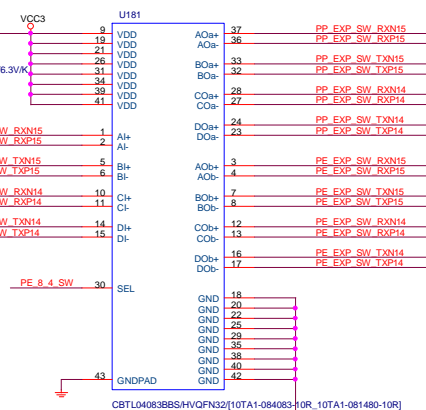
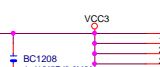


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GIGABYTE™			
Title			
PCIE_X1 1,2,3			
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<u>PA EXP SW_RXIP[8..15]</u>	→ PA_EXP_SW_RXIP[8..15]	15
<u>PA EXP SW_RXIN[8..15]</u>	→ PA_EXP_SW_RXIN[8..15]	15
<u>PA EXP SW_TXIP[8..15]</u>	→ PA_EXP_SW_TXIP[8..15]	15
<u>PA EXP SW_TXIN[8..15]</u>	→ PA_EXP_SW_TXIN[8..15]	15
<u>PE EXP SW_RXIP[8..15]</u>	→ PE_EXP_SW_RXIP[8..15]	16
<u>PE EXP SW_RXIN[8..15]</u>	→ PE_EXP_SW_RXIN[8..15]	16
<u>PE EXP SW_TXIP[8..15]</u>	→ PE_EXP_SW_TXIP[8..15]	16
<u>PE EXP SW_TXIN[8..15]</u>	→ PE_EXP_SW_TXIN[8..15]	16

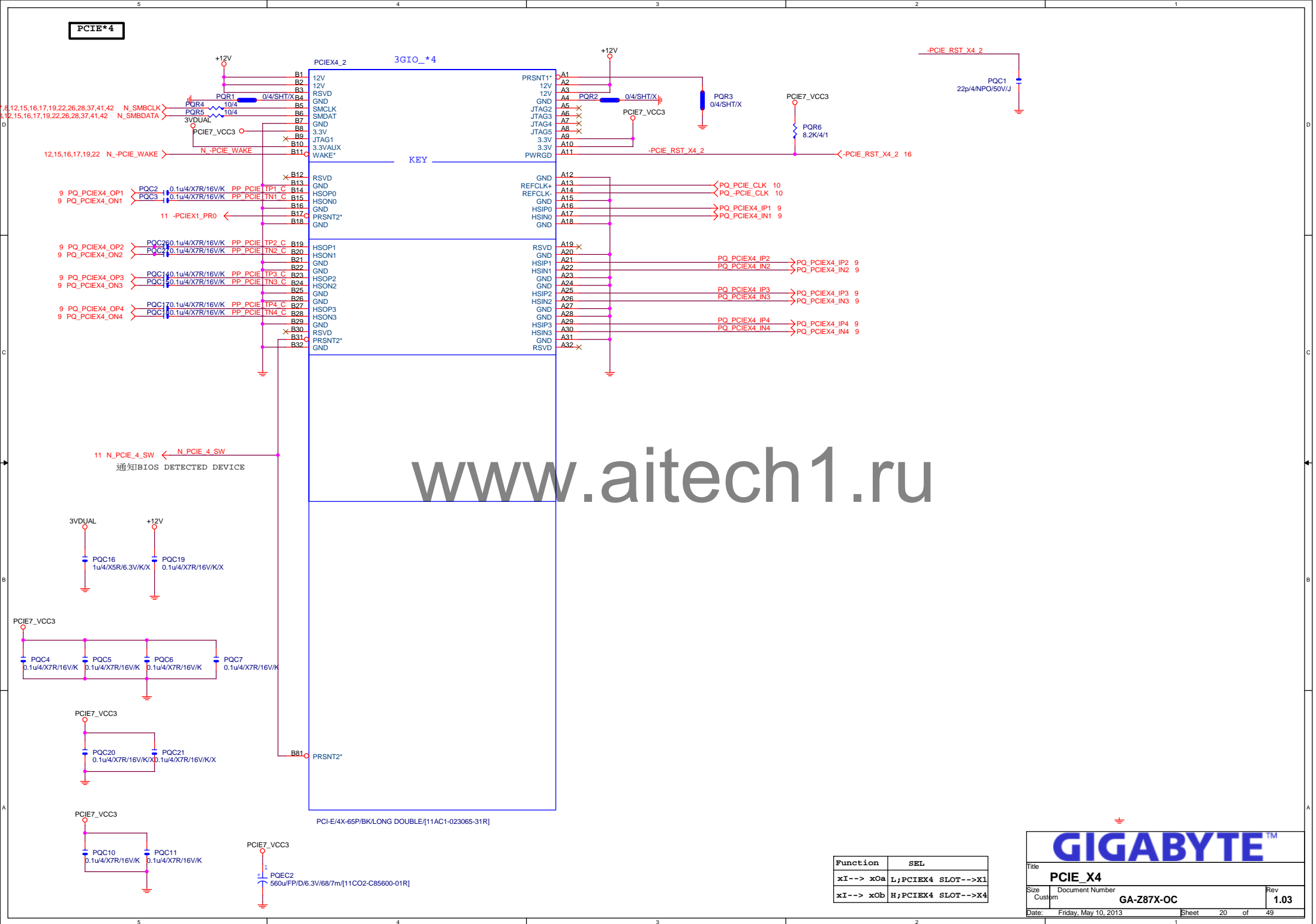


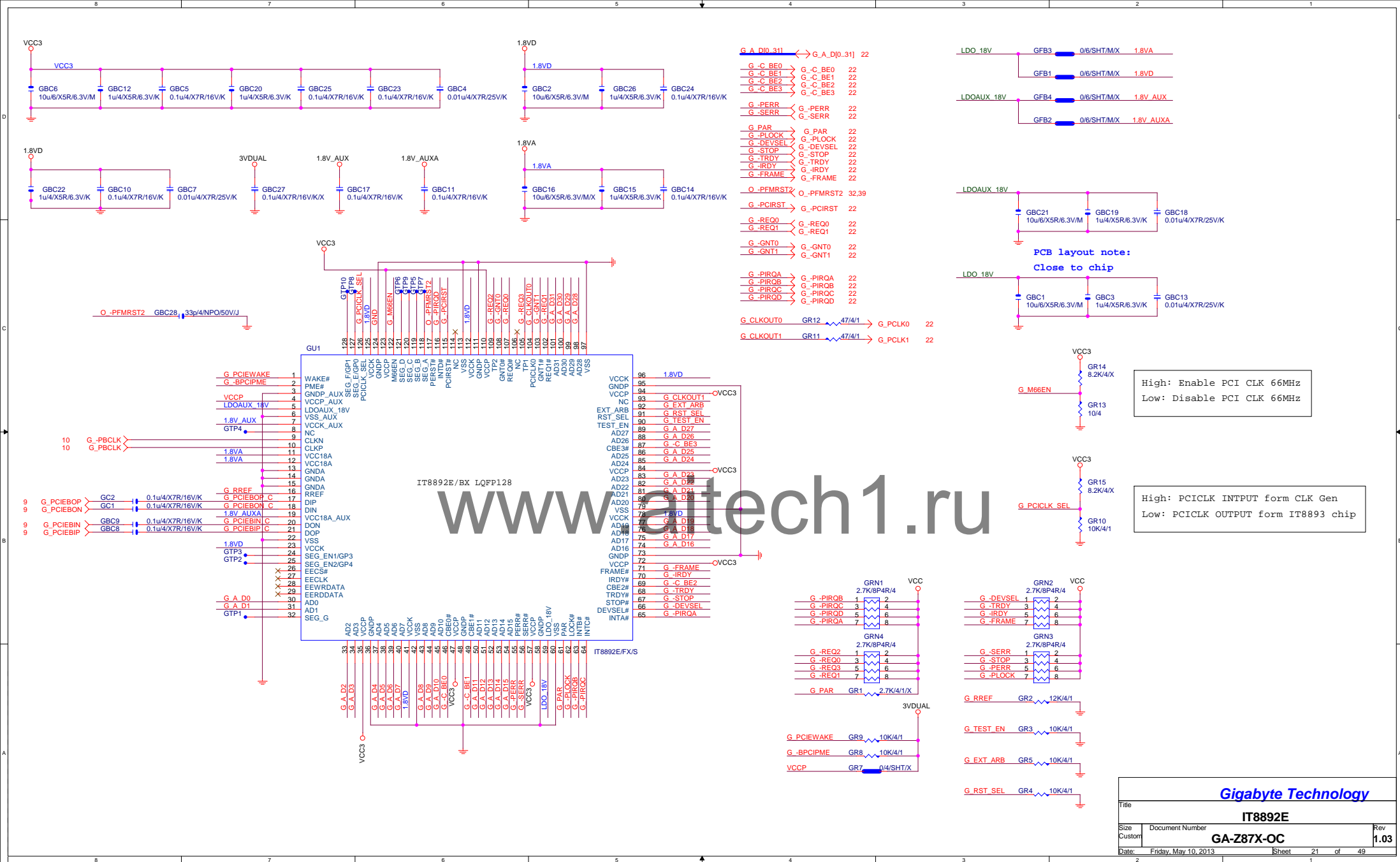
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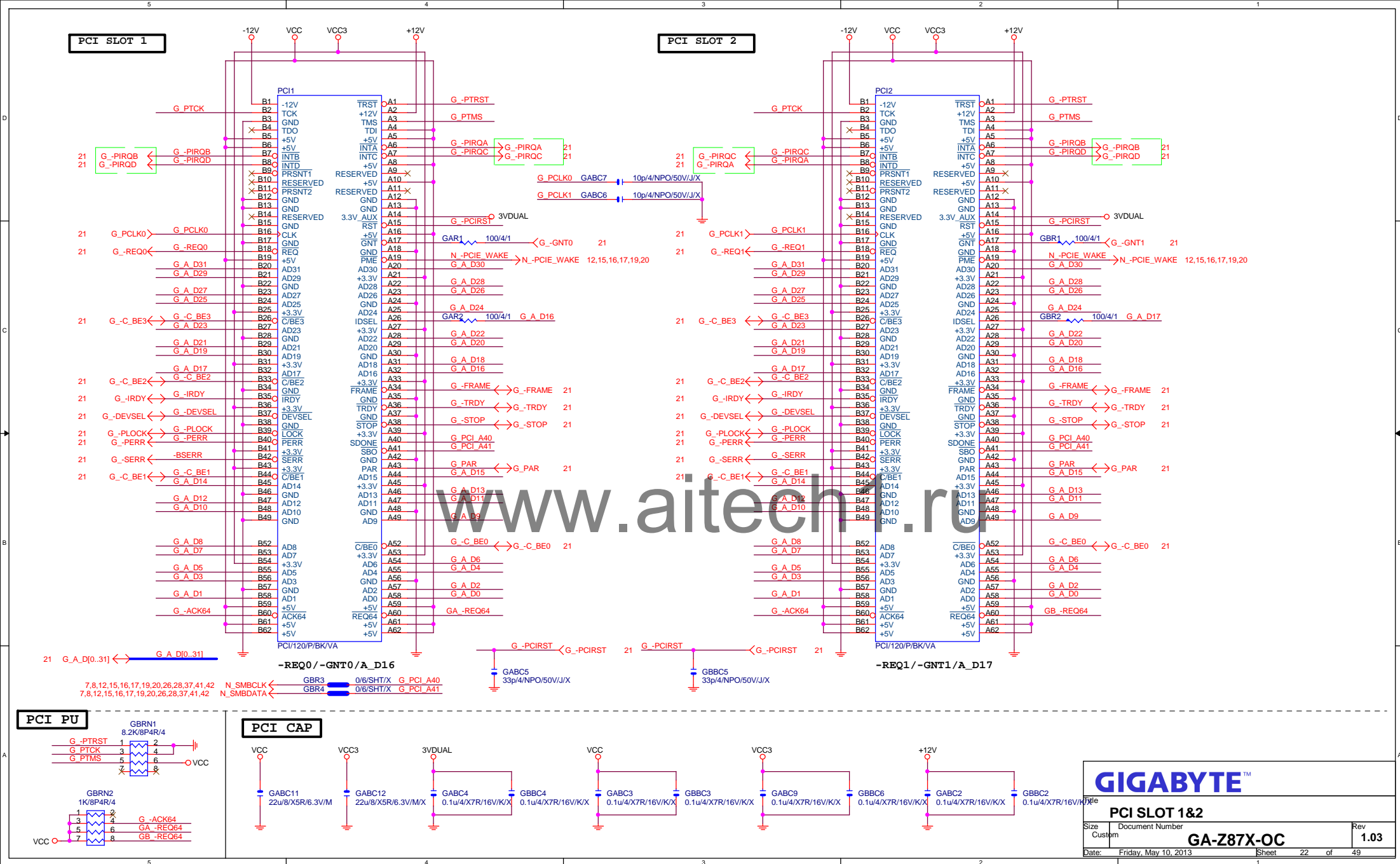
PP_EXP_SW_RXP[12..15] >> PP_EXP_SW_RXP[12..15] 19
PP_EXP_SW_RXN[12..15] >> PP_EXP_SW_RXN[12..15] 19
PP_EXP_SW_TXP[12..15] >> PP_EXP_SW_TXP[12..15] 19
PP_EXP_SW_TXN[12..15] >> PP_EXP_SW_TXN[12..15] 19

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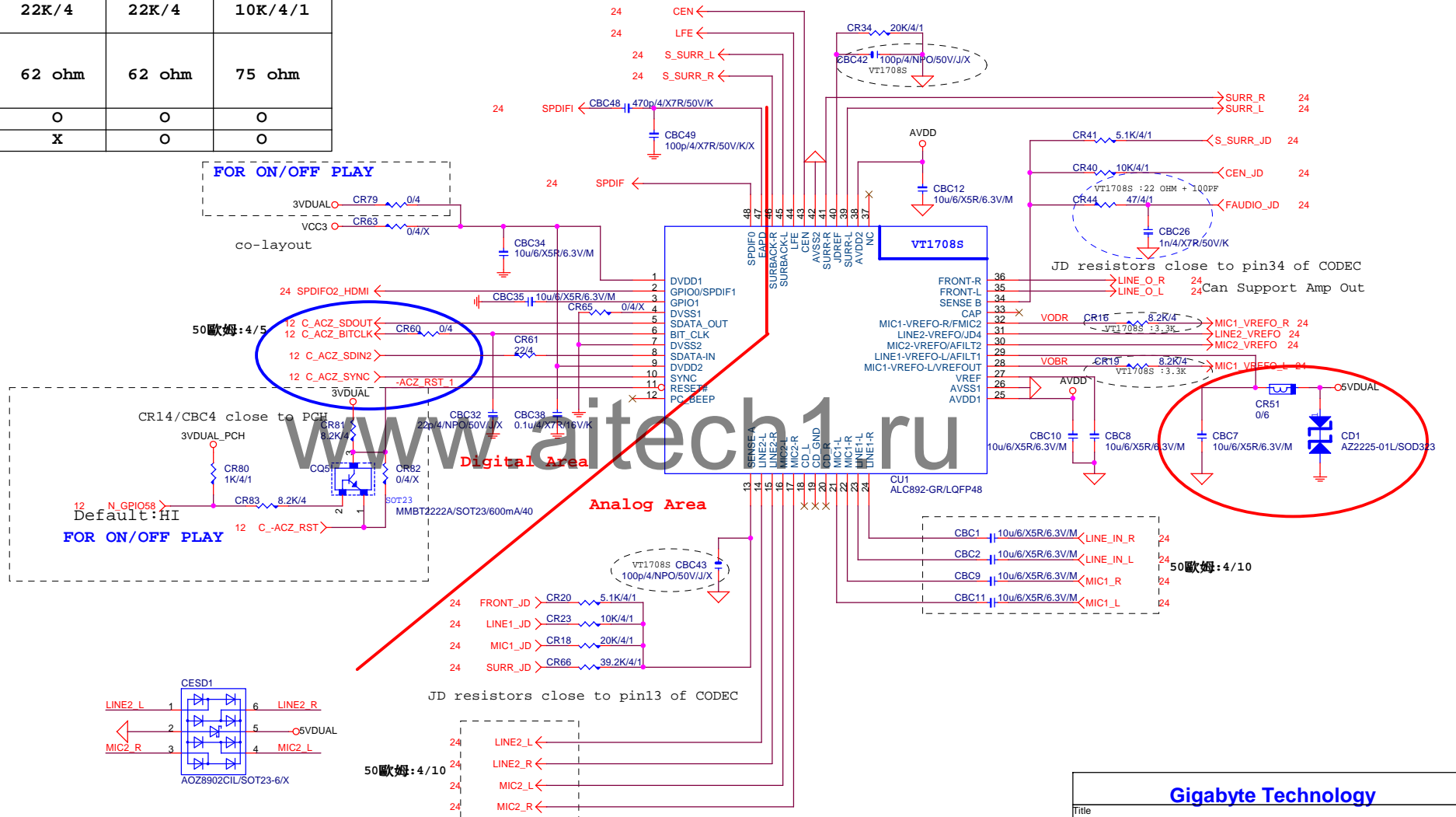
Function	SEL
xI--> x0a	L
xI--> x0b	H

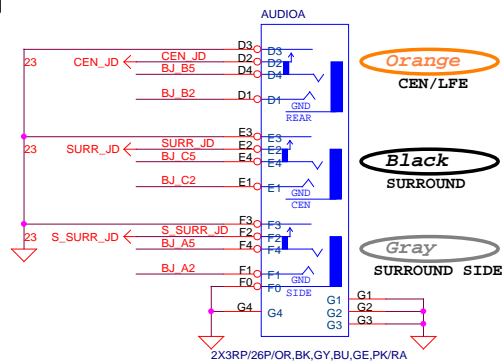
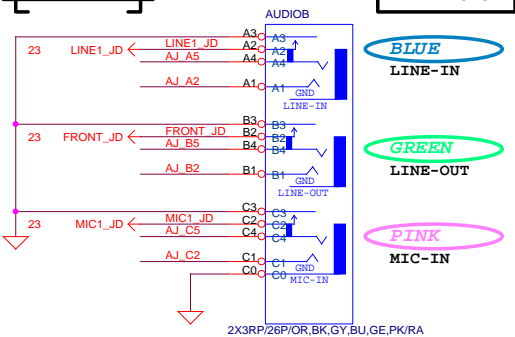
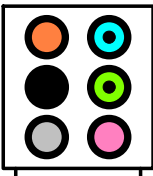
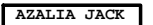
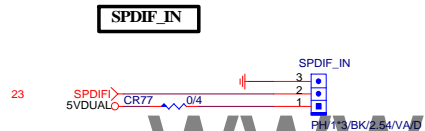
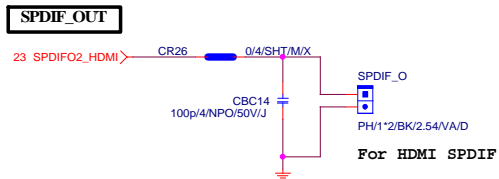
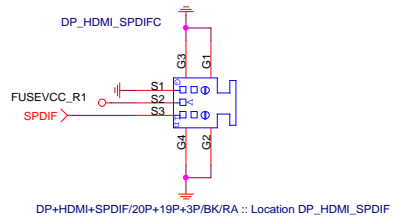
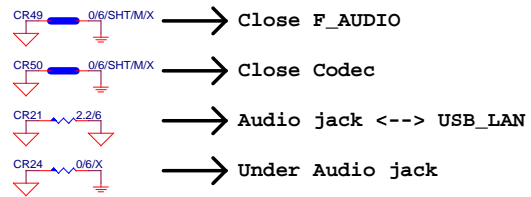




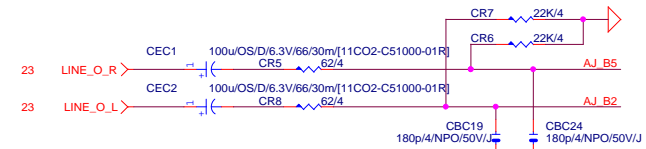


	ALC892	ALC887-VD2	VT1708S-CE
CR44/CBC26	47ohm+1nF	47ohm+1nF	22ohm+100P
CBC42/CBC43	X	X	100P/4
CR16/CR19 CR52/CR56/CR10/CR9	8.2K/4	8.2K/4	3.3K/4/1
CR6/CR7/CR58/CR54/ CR67/CR68/CR69/CR70	22K/4	22K/4	10K/4/1
CR5/CR8/CR1/CR14/ CR17/CR22/CR73/CR74/ CR13/CR11/CR57/CR53/ CR75/CR76	62 ohm	62 ohm	75 ohm
CR51/CD1/CBC7	O	O	O
CESD1	X	O	O



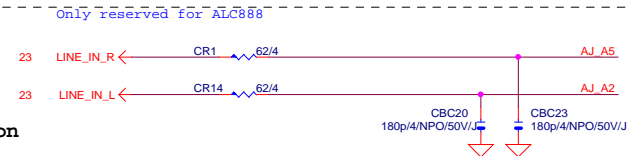


LINE-OUT

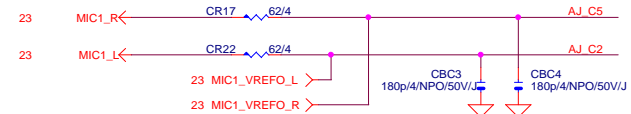


LINE-IN

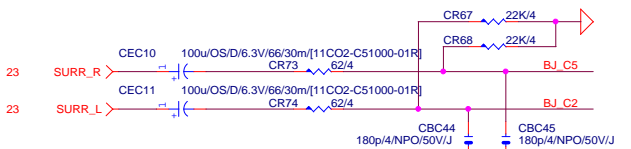
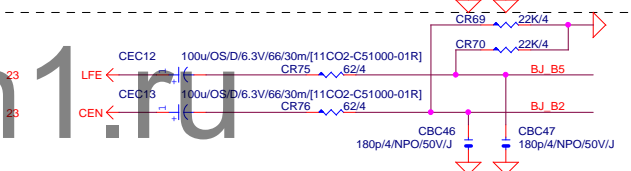
Verify MIC function
in LINE-in



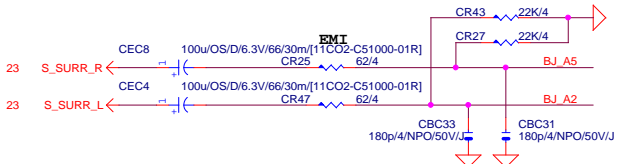
For 889A/888

MIC-IN

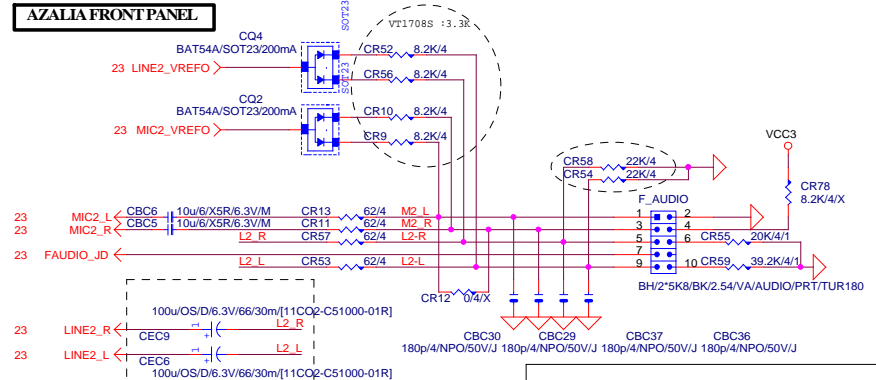
SURROUND

**CEN/LFE**

SURR BACK



AZALIA FRONT PANEL



Gigabyte Technology

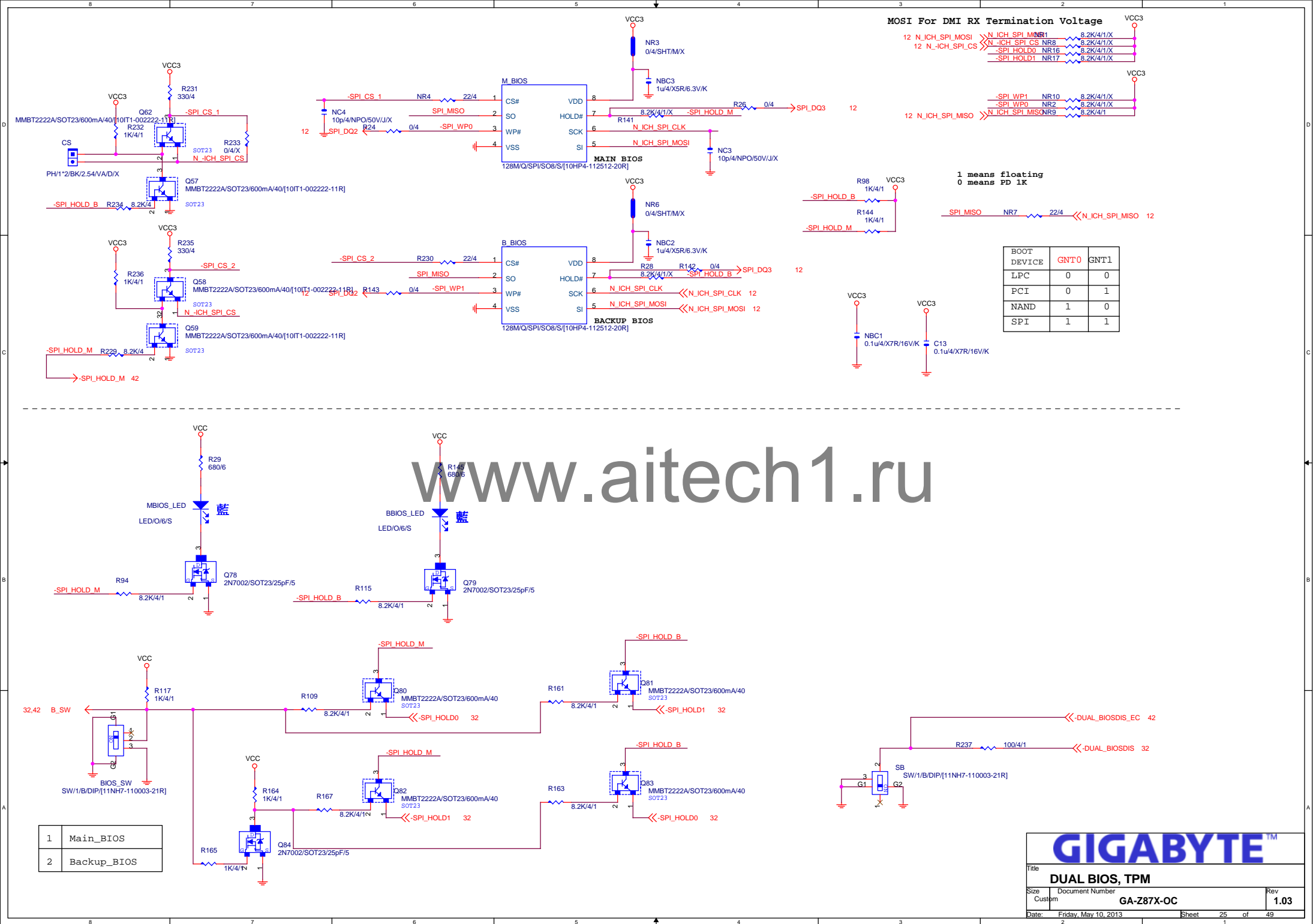
AUDIO JACK

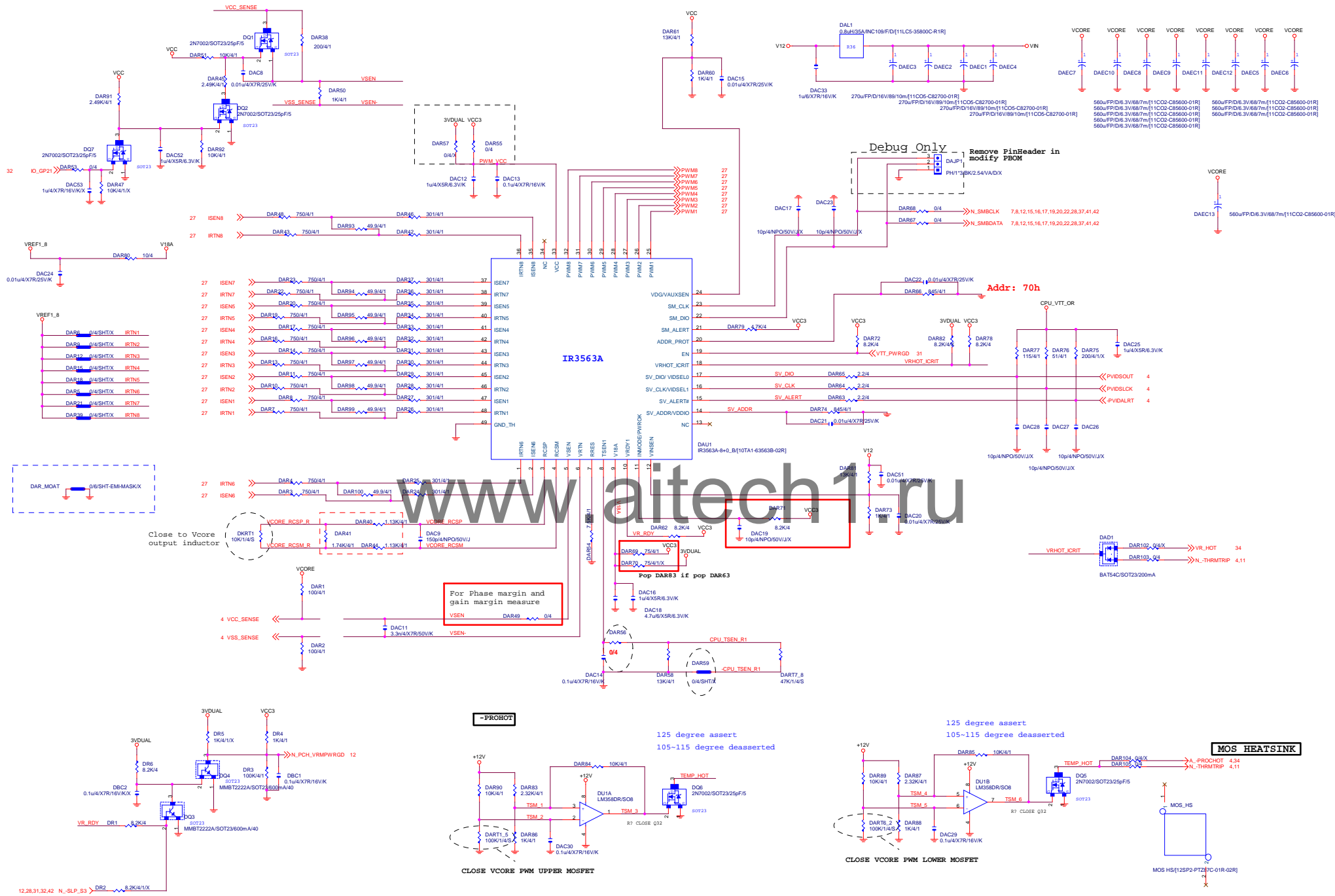
GA-Z87X-OC

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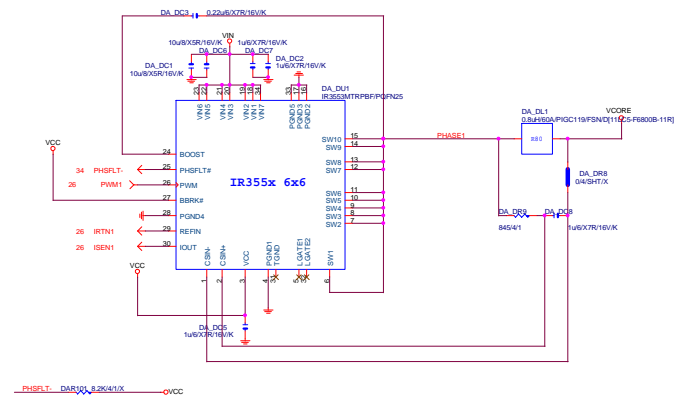
Date: Friday, May 10, 2013

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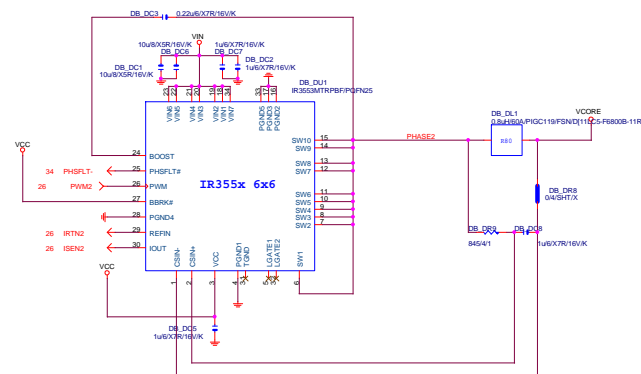




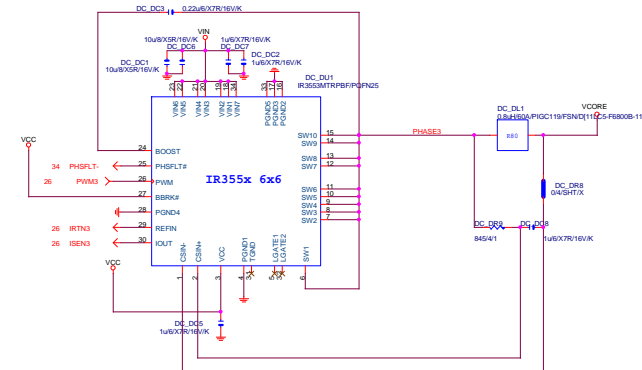
VCORE-PHASE1



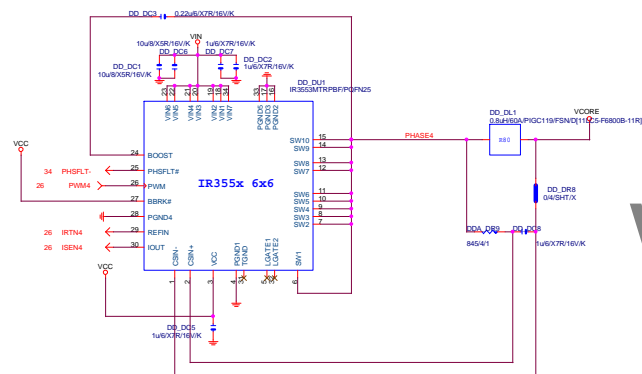
VCORE-PHASE2



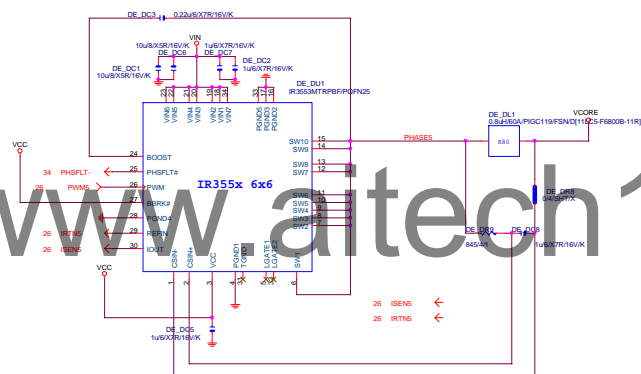
VCORE-PHASE3



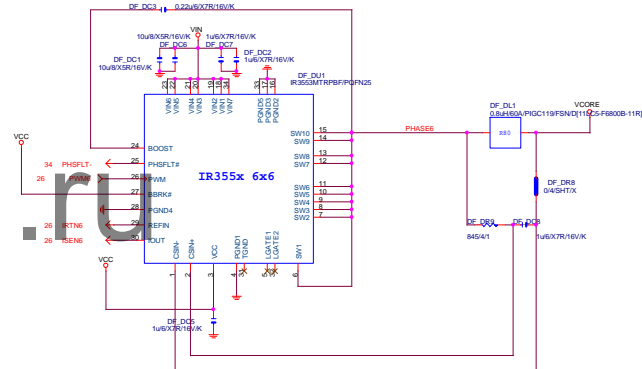
VCORE-PHASE4



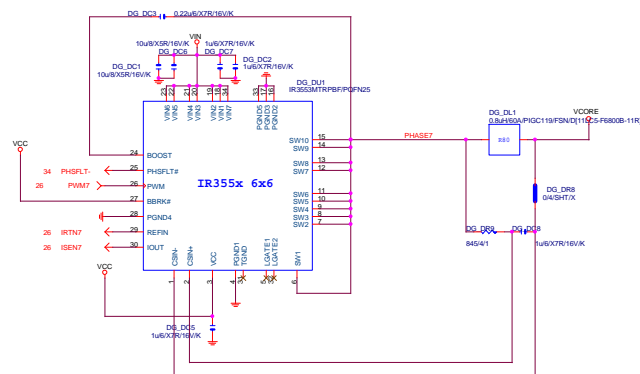
VCORE-PHASE5



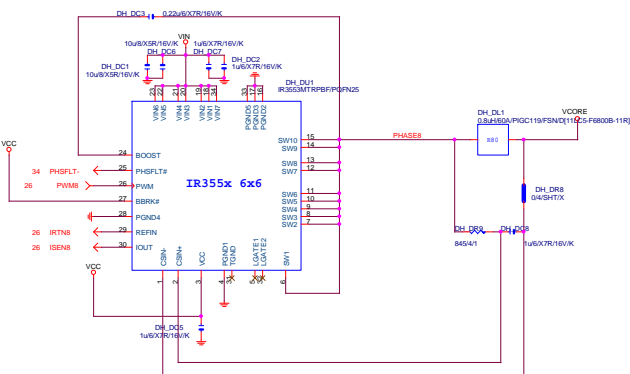
VCORE-PHASE6

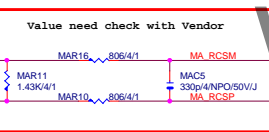
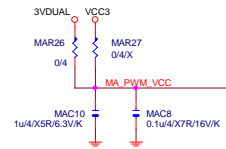
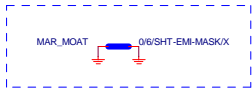


VCORE-PHASE7



VCORE-PHASE8

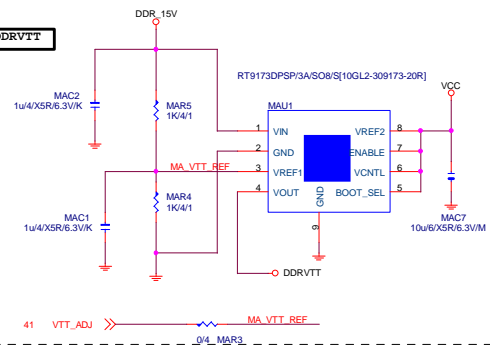




Close to DDR output inductor

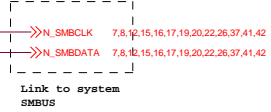
should be routed as differential pair, 7mil width, 8mil spacing

DDRVTT



IR3570

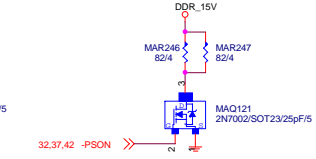
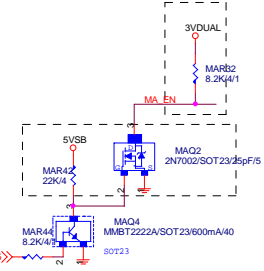
MA_PWM2 29
MA_PWM1 29



Addr: 72h

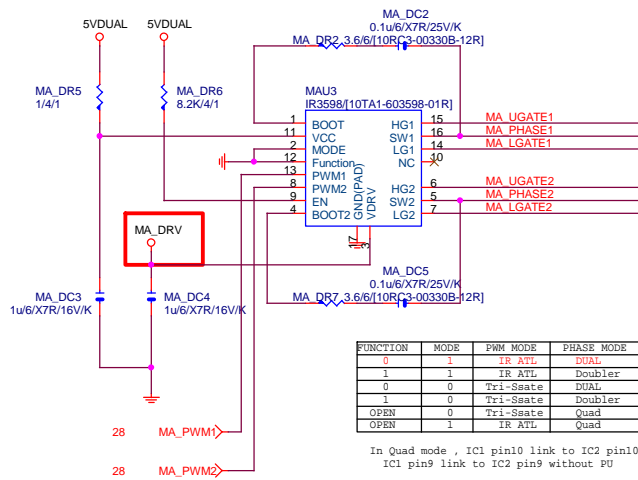
Link to PCH pin BQ46

Full up in PCH side



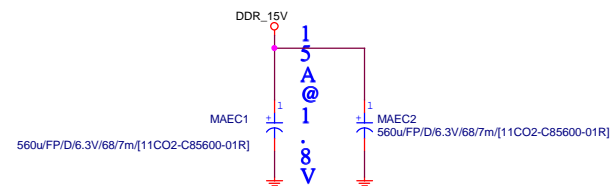
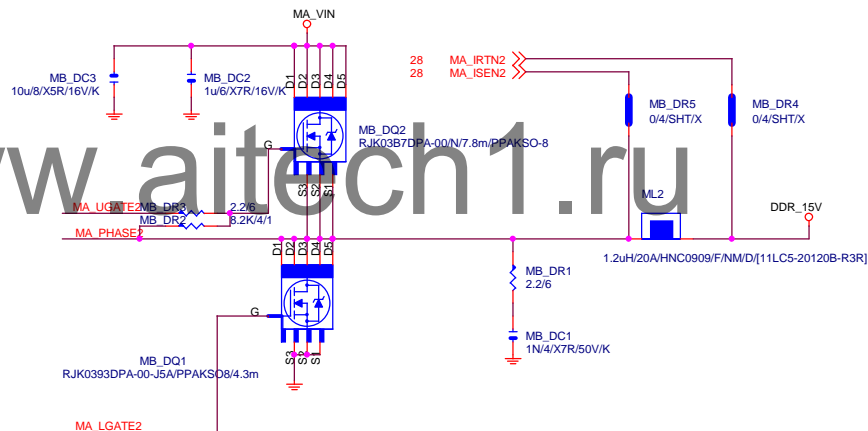
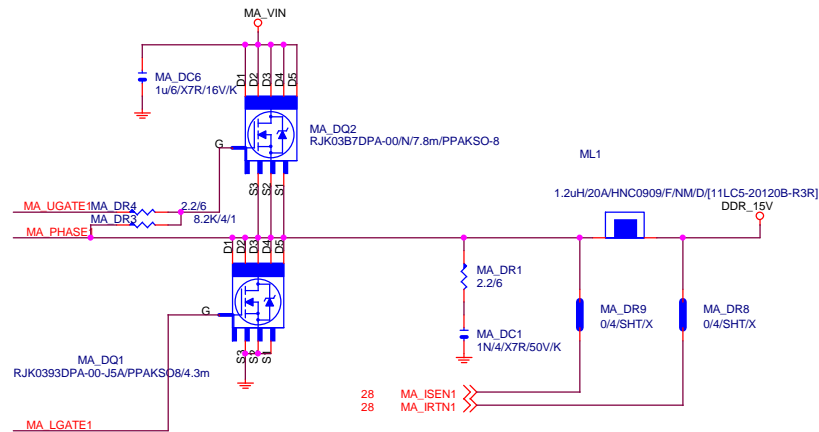
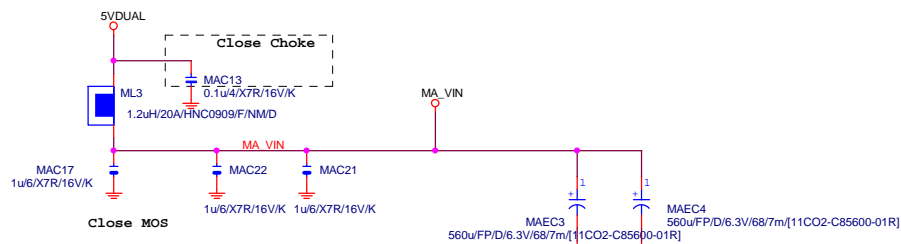
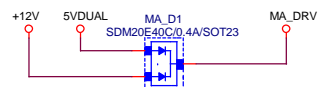
GIGABYTE™		
Title DDR POWER IR3570		
Size C	Document Number GA-Z87X-OC	Rev 1.03
Date: Friday, May 10, 2013	Sheet 28	of 49

DDR_15V

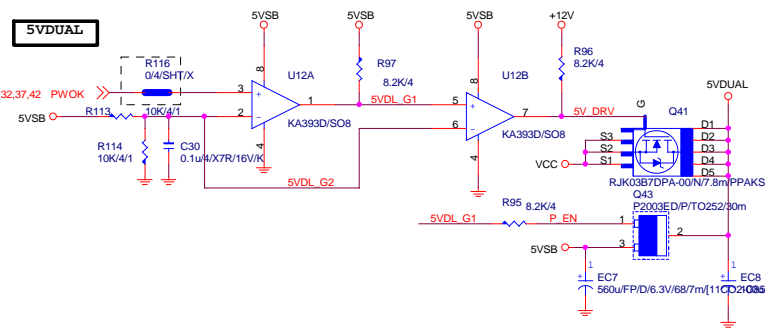


FUNCTION	MODE	PWM MODE	PHASE MODE
0	1	IR ATL	DUAL
1	1	IR ATL	Doubler
0	0	Tri-Ssate	DUAL
1	0	Tri-Ssate	Doubler
OPEN	0	Tri-Ssate	Quad
OPEN	1	IR ATL	Quad

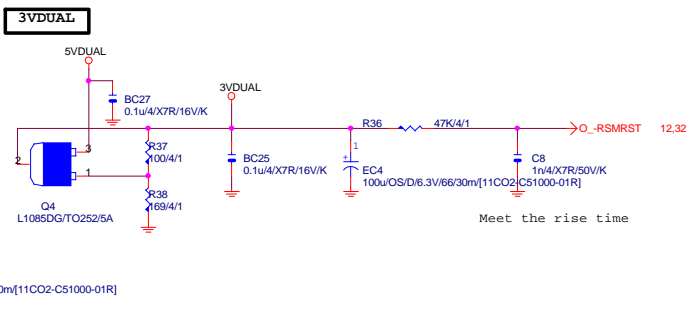
In Quad mode , IC1 pin10 link to IC2 pin10
IC1 pin9 link to IC2 pin9 without PU



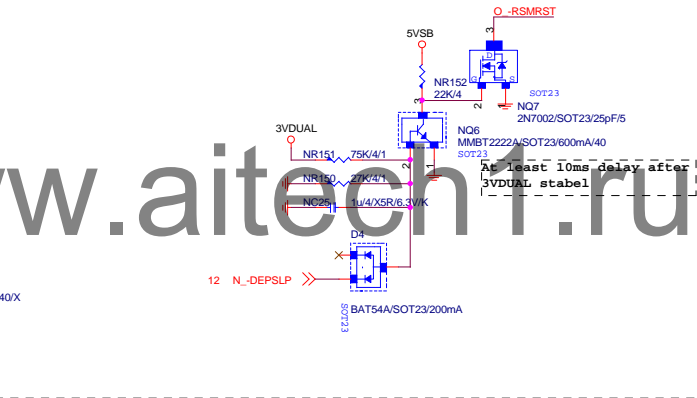
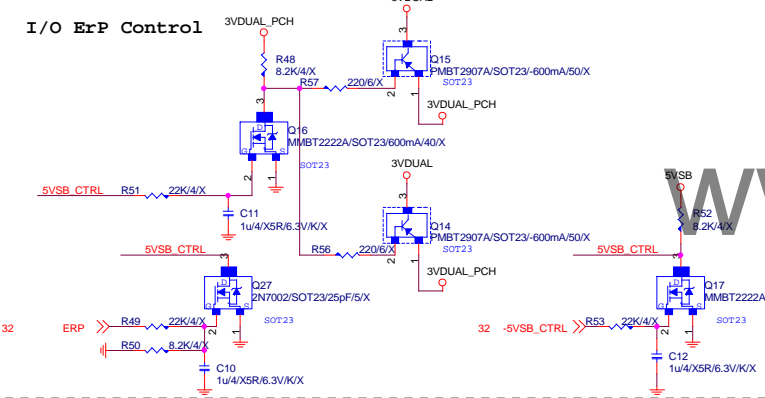
5VDUAL



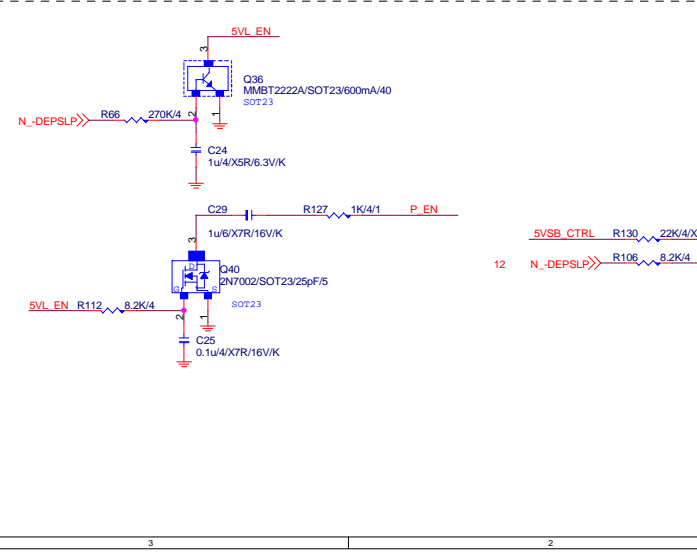
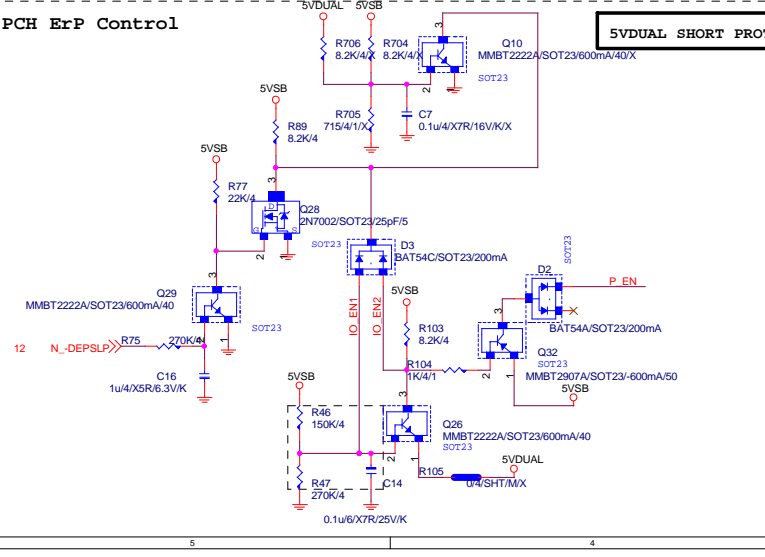
3VDUAL



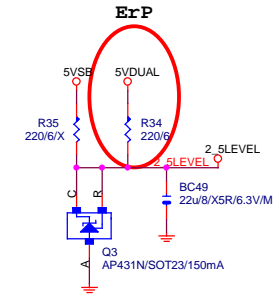
I/O ErP Control

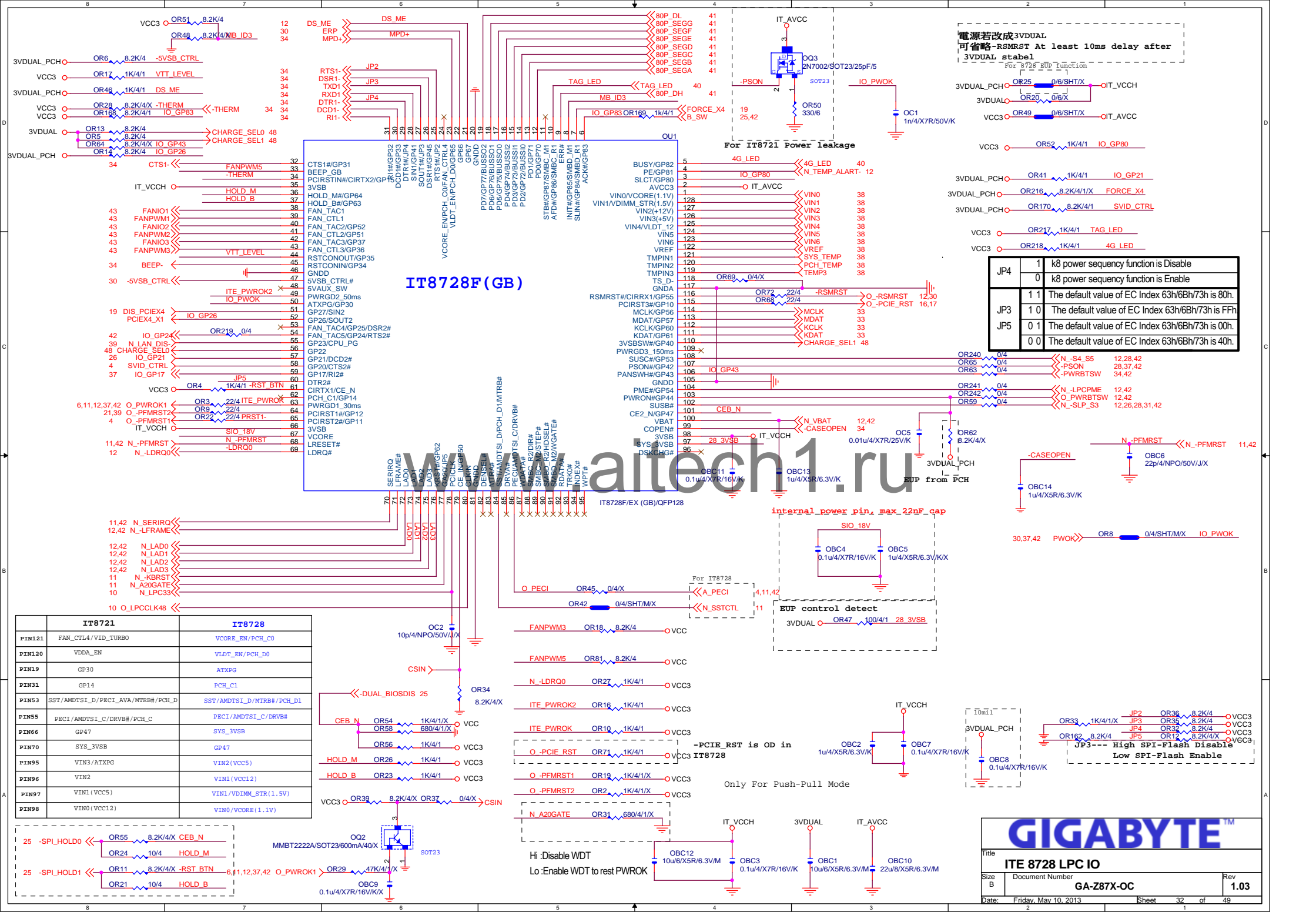


PCH ErP Control

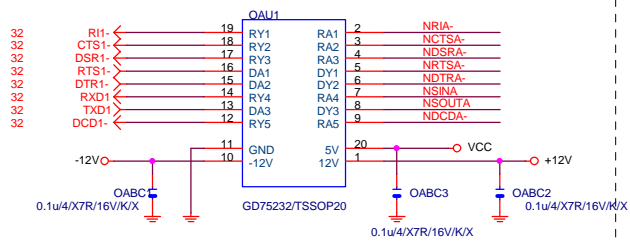


The schematic diagram illustrates the VCC1_05 power plane. It features a voltage regulator (U6C, LM324DR) powered by a +12V supply. The regulator's output (pin 8) provides VCC1_05_G, which is connected to the power pins (D1, D2, D3, D4, D5) of two DDR3 memory modules (NQ16 and NQ15). The regulator is also connected to a feedback network consisting of resistors R191, R192, R199, and R198. A decoupling capacitor C80 is connected between the regulator's output and ground. The power plane is connected to the VCC1_05_PCH pin of the processor (41) and the VCC1_05_PCH pin of the NEC3 component. The NEC3 component is connected to ground via a capacitor (560uF/FP/D/6.3V/68/7m[11CO2-C85600-01R]).

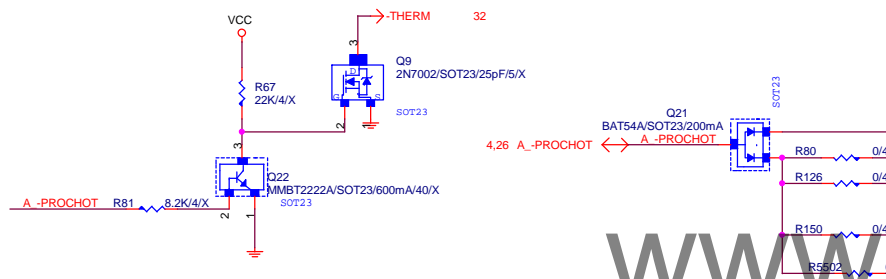
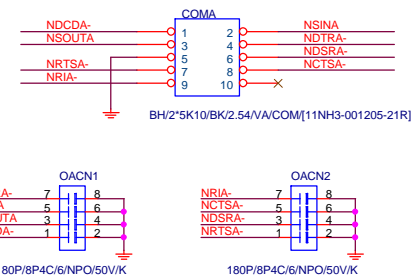
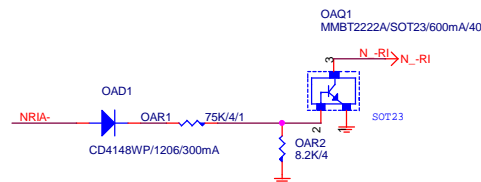
[illegible]



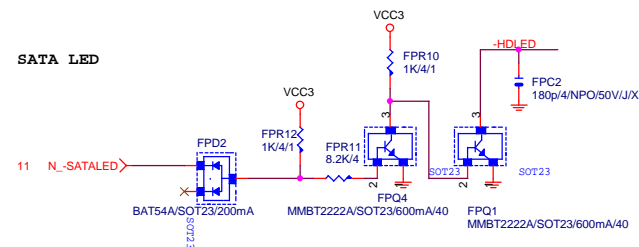
COMA



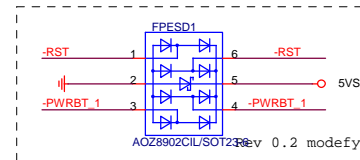
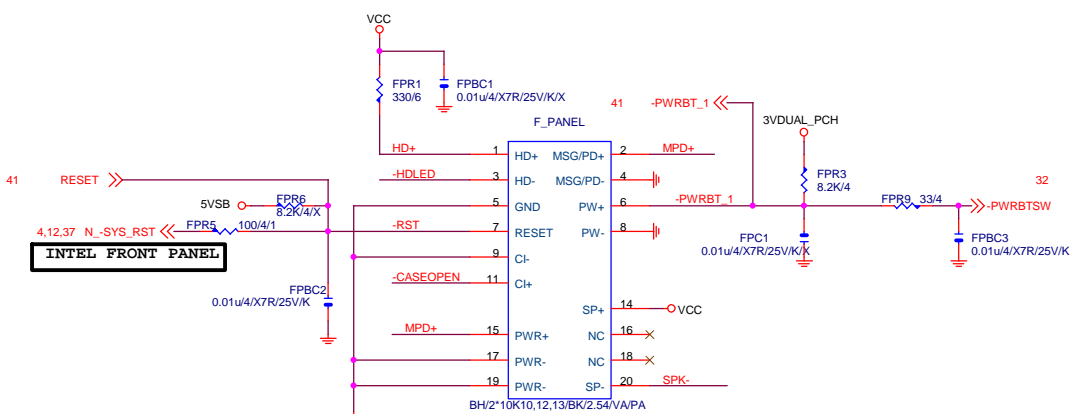
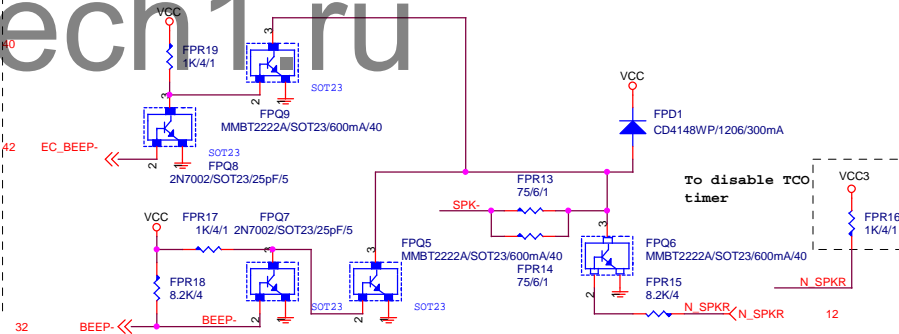
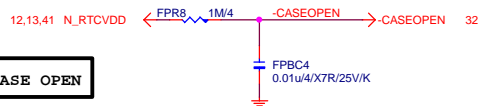
COM RI



SATA LED



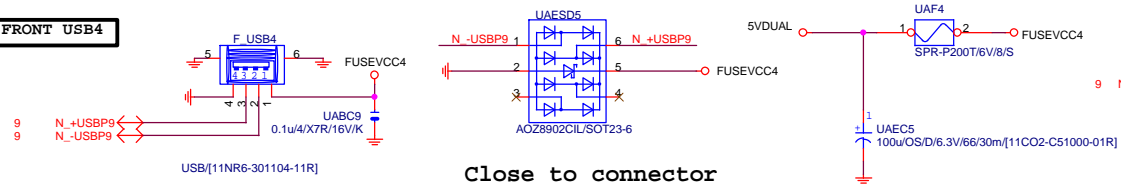
CASE OPEN



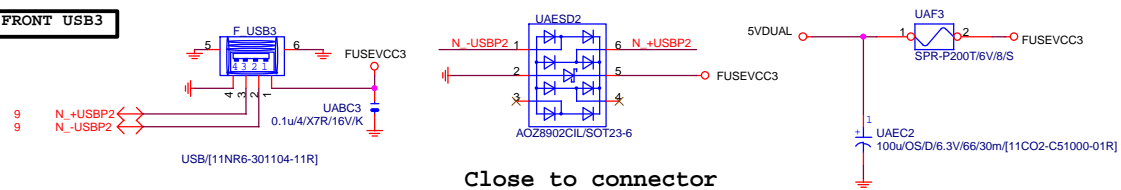
Close to connector

GIGABYTE™			
Title FP, COM, -PHOT			
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	2	1	

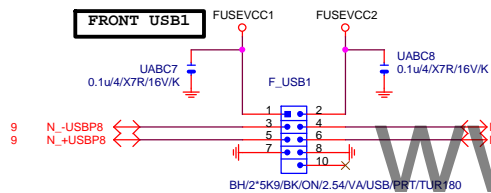
FRONT USB4



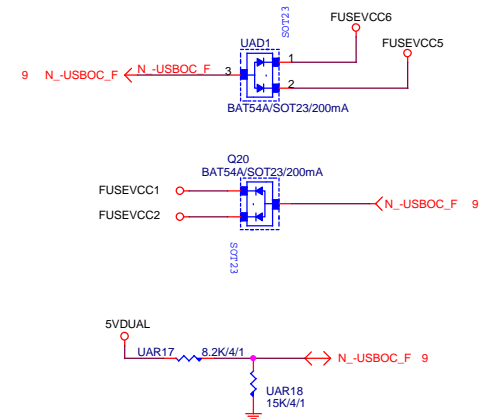
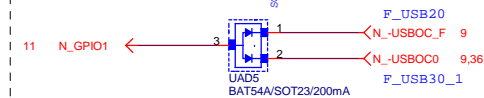
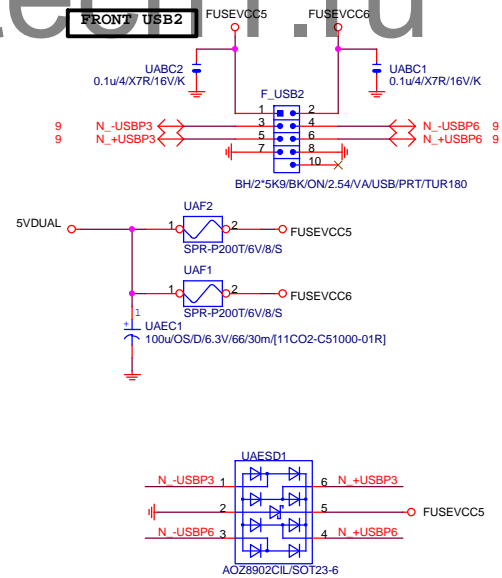
FRONT USB3



FRONT USB1

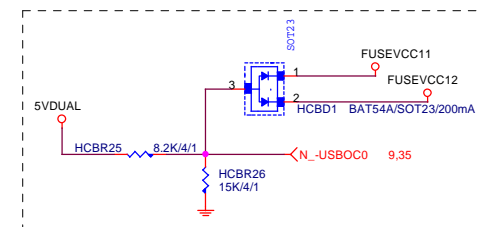
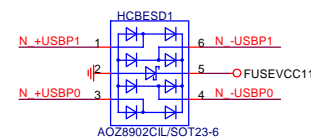
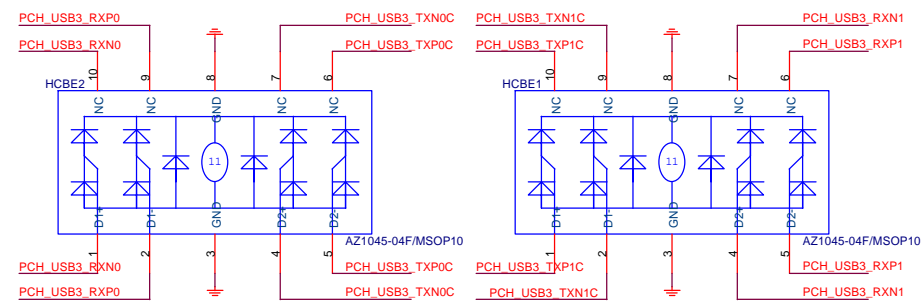


FRONT USB2



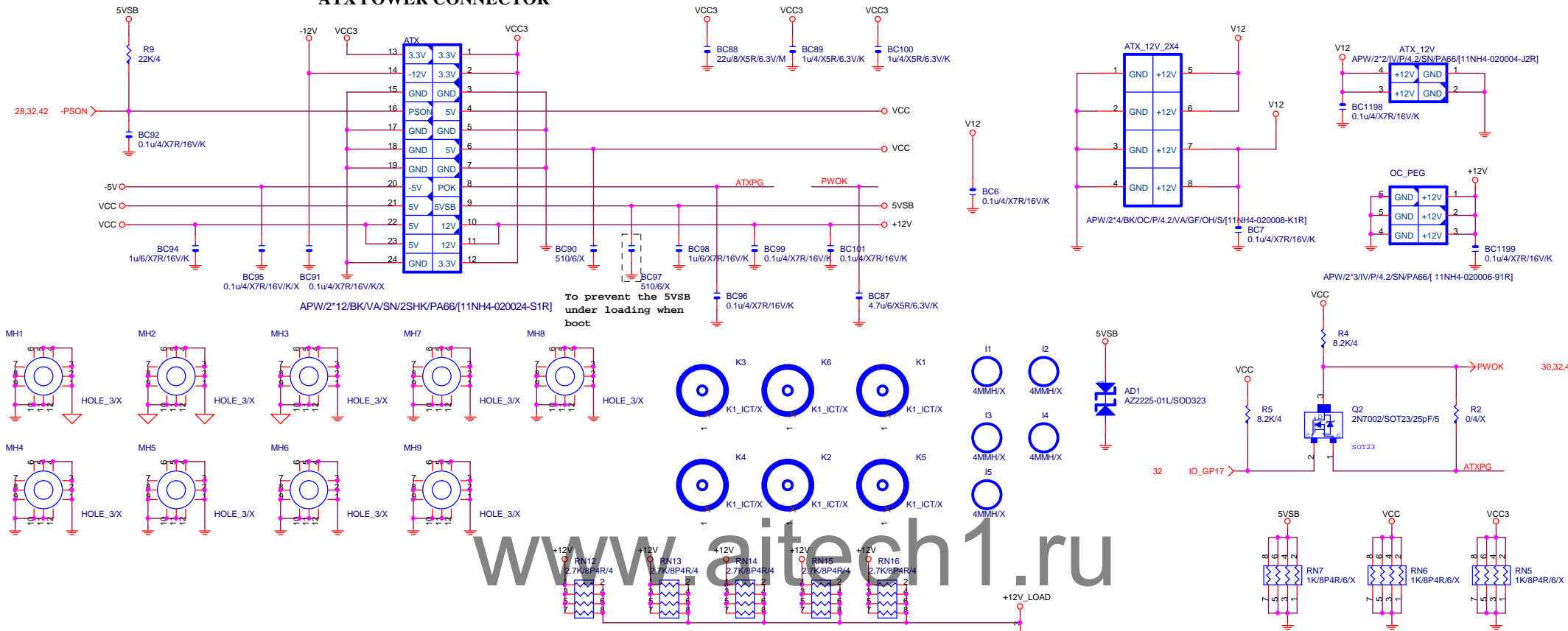
GIGABYTE™

Title FRONT USB 2.0		
Size Custom	Document Number GA-Z87X-OC	Rev 1.03
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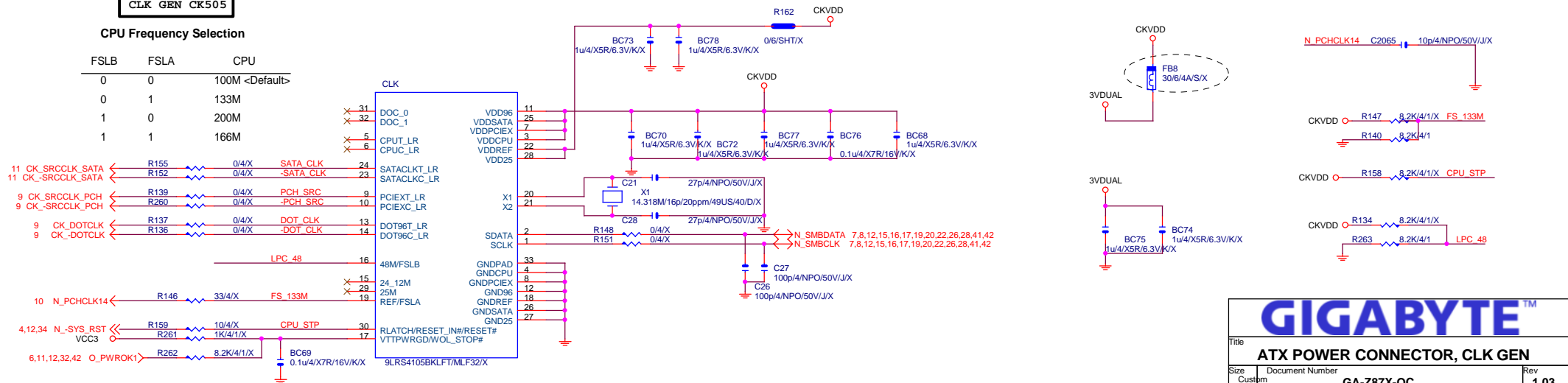
ATX POWER CONNECTOR



CLK GEN CK505

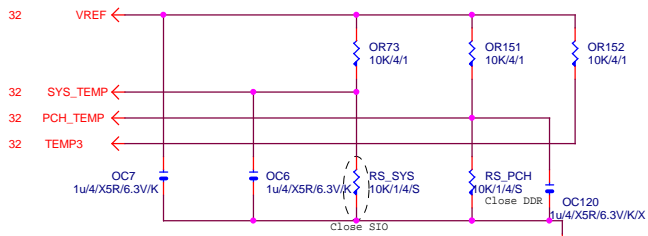
CPU Frequency Selection

FSLB	FSLA	CPU
0	0	100M <Default>
0	1	133M
1	0	200M
1	1	166M

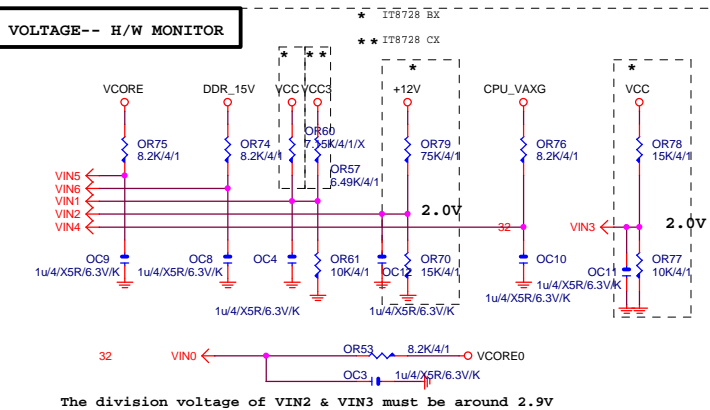
**GIGABYTE™**

Title			
ATX POWER CONNECTOR, CLK GEN			
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Custom	GA-Z87X-OC	1.03	
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TEMP H/W MONITOR



VOLTAGE-- H/W MONITOR

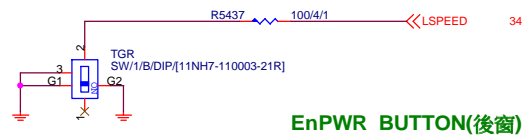


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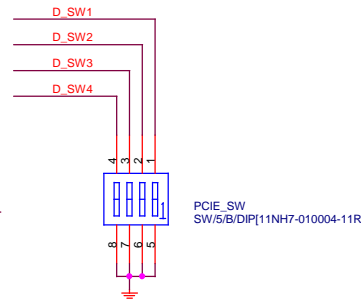
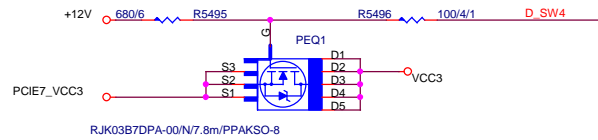
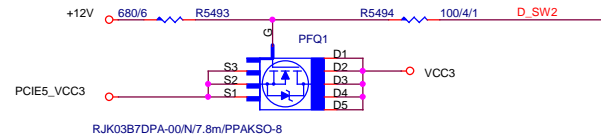
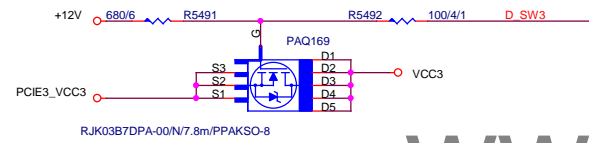
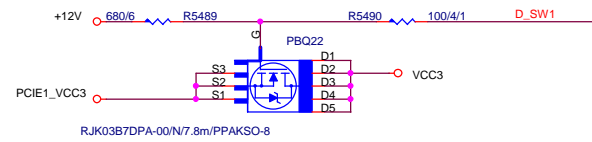
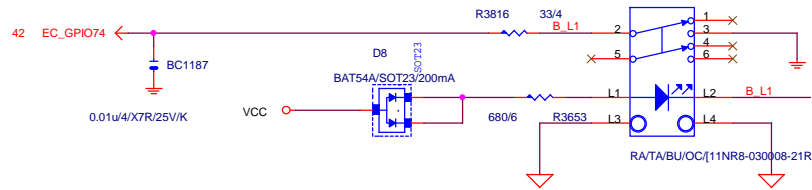
GIGABYTE™

Title			HWM, FAN CTRL	
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Rev	1.03			

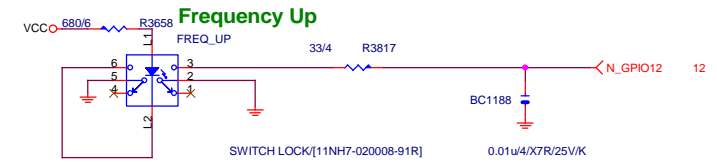
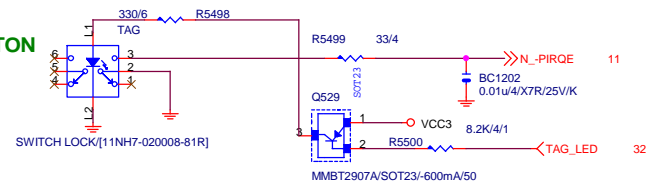
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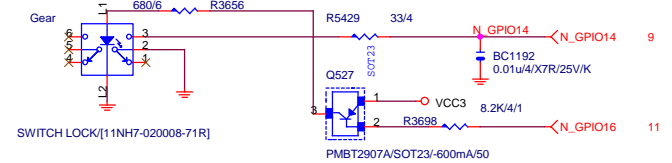
OC_IGNITION



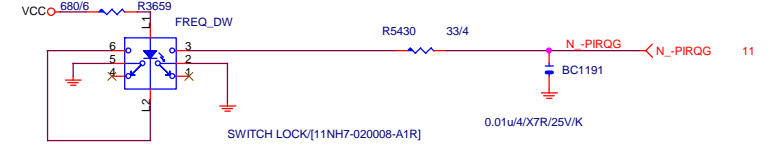
TAG BUTTON



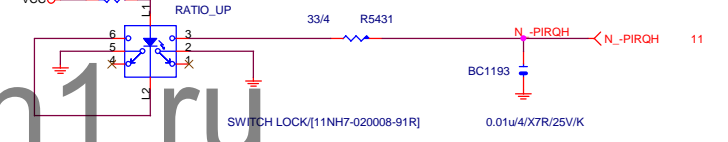
Gear



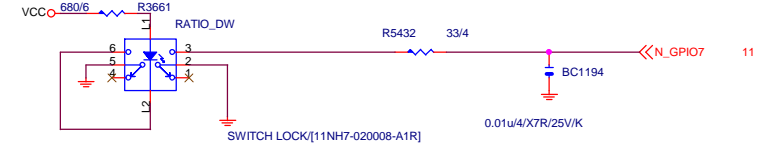
Frequency Down



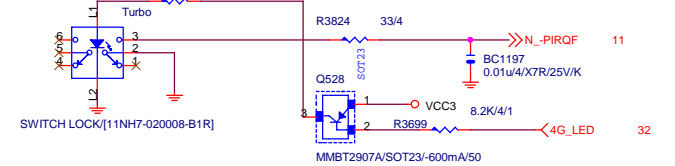
Ratio Up



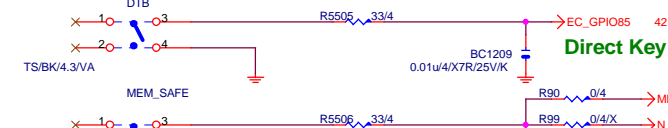
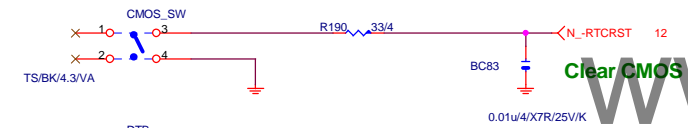
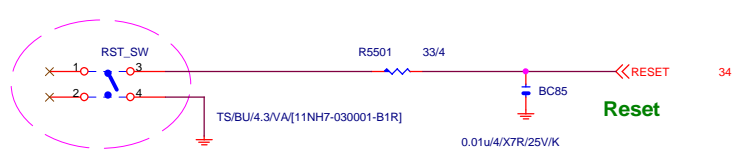
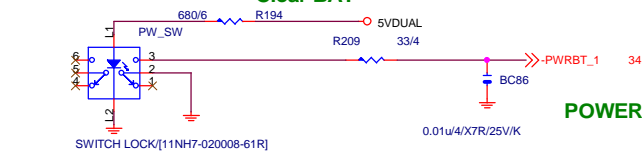
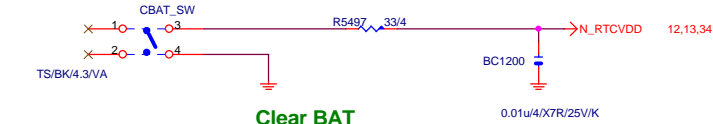
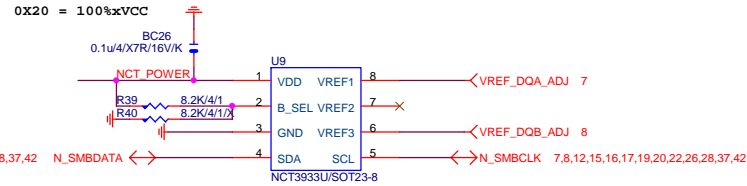
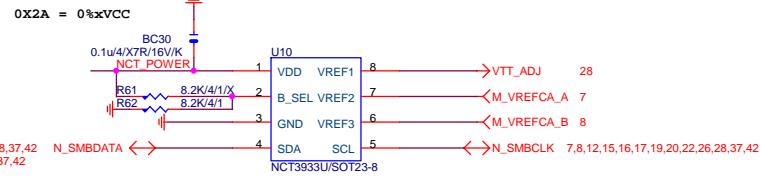
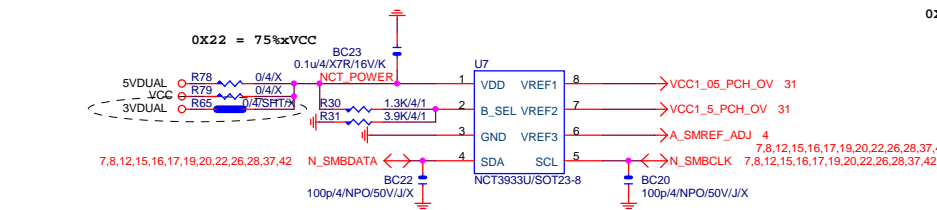
Ratio Down



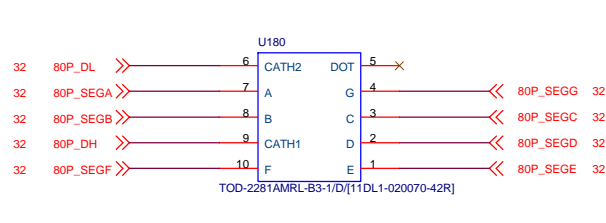
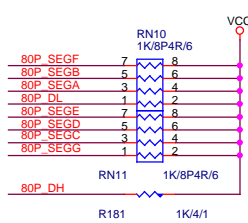
Turbo



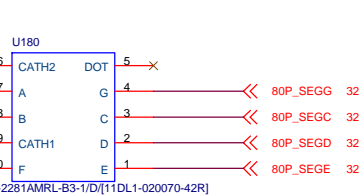
GIGABYTE™			
Title SWITCH			
Size	Document Number	Rev	
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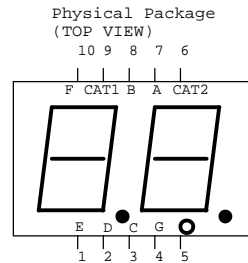
80 PORT



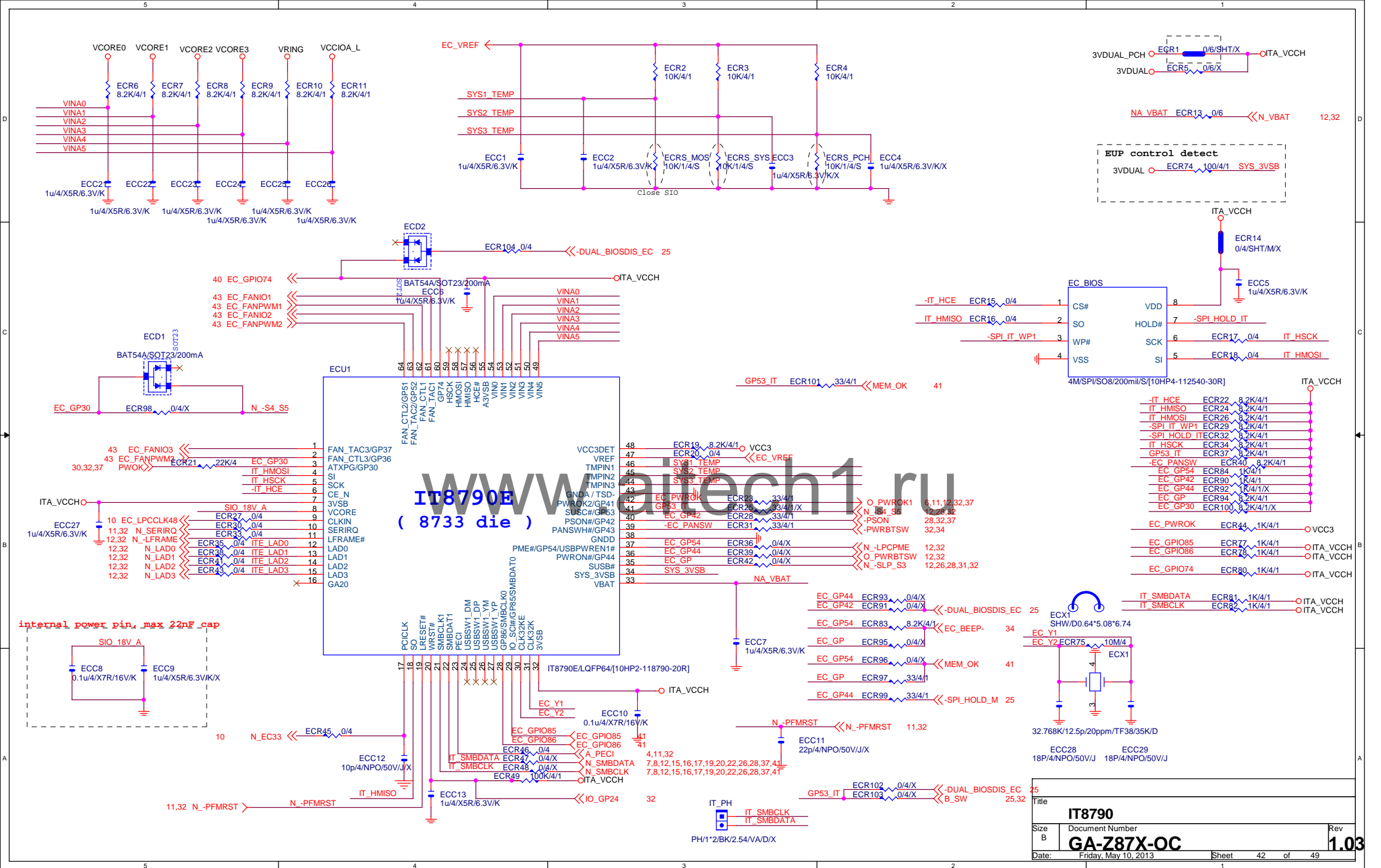
COMMON CATHODE



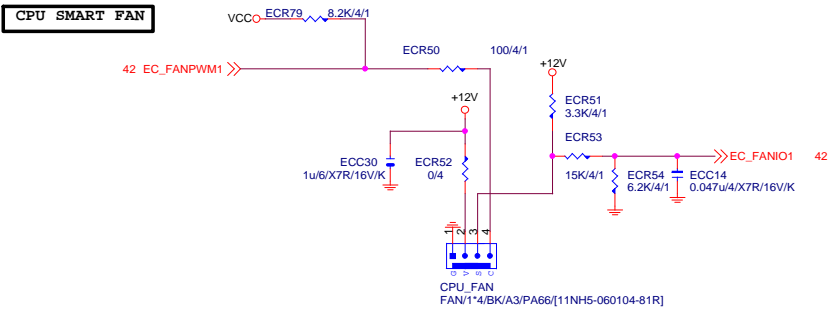
COMMON CATHODE



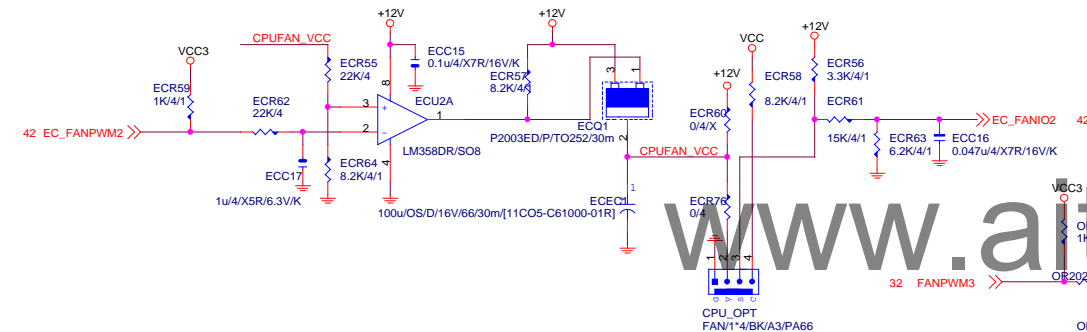
GIGABYTE™			
Title			
RST, PWR, CLR_CMOS, OV			
Size	Document Number	Rev	
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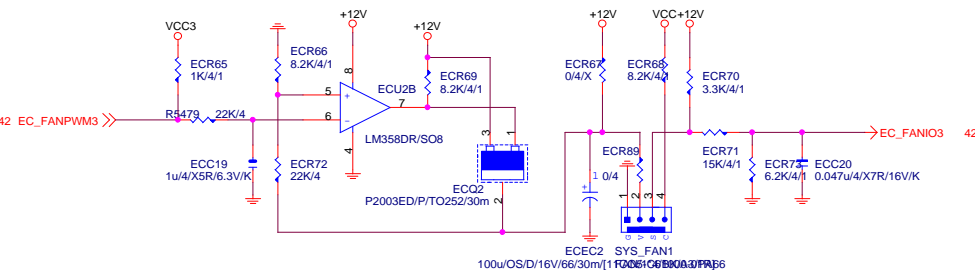
CPU SMART FAN



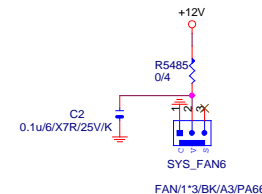
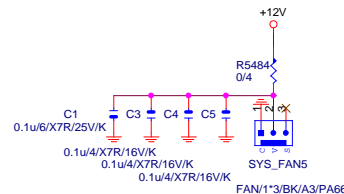
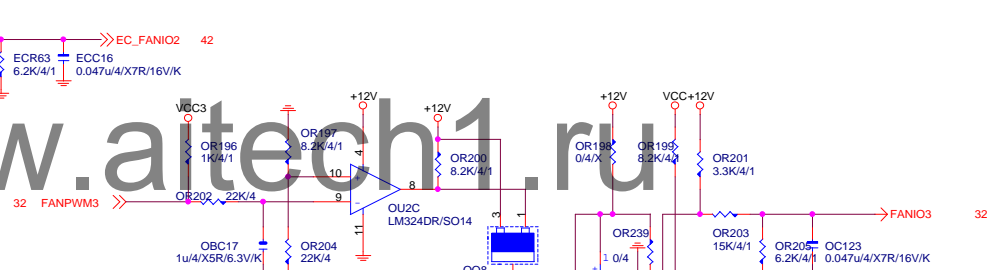
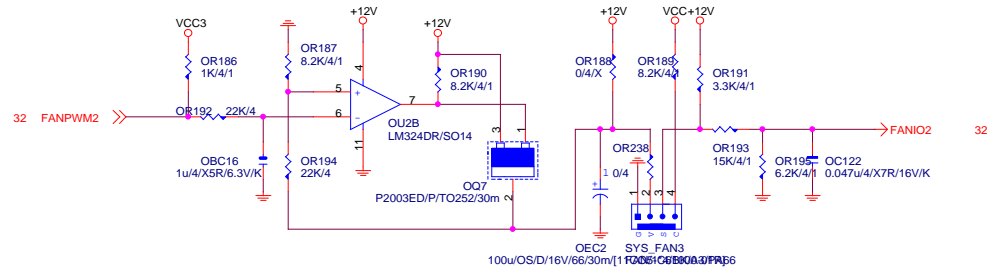
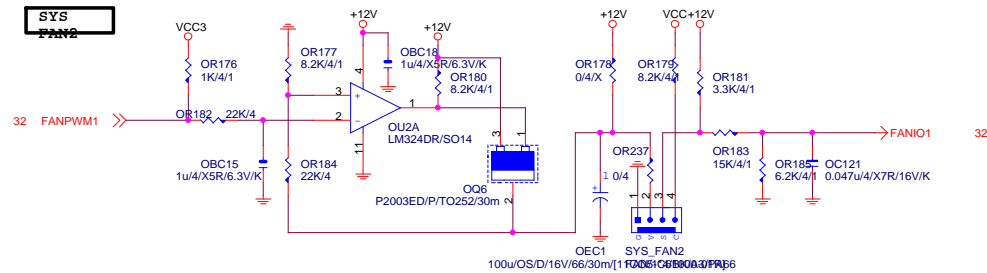
CPUOPT FAN



SYS FAN1

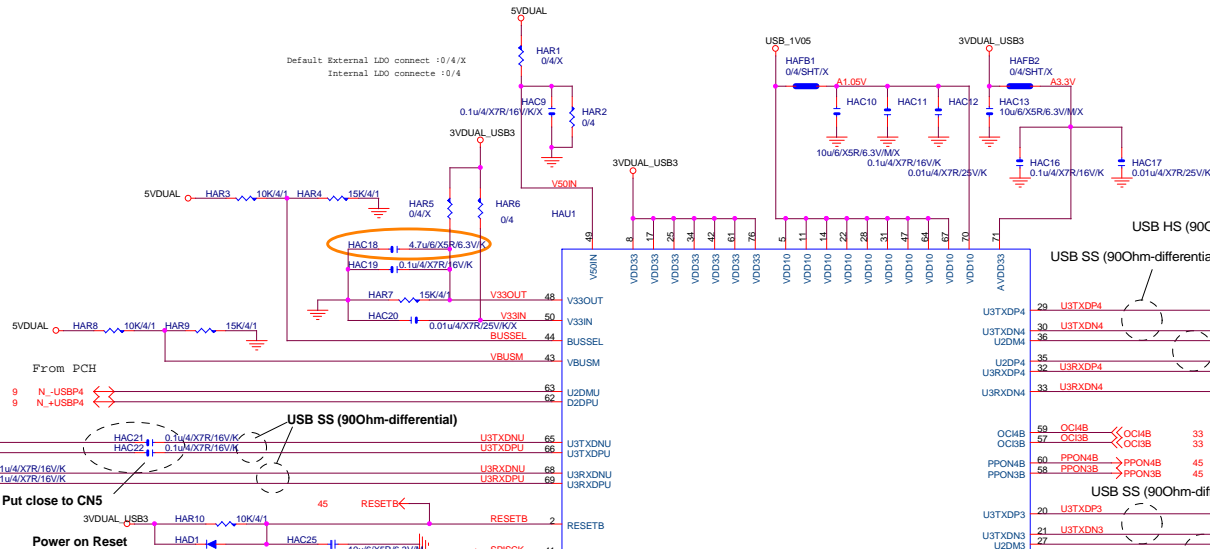
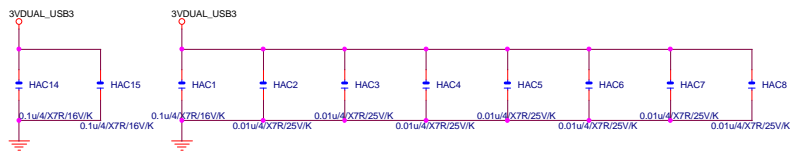


SYS FAN2



Gigabyte Technology

Title			HWM,KB/MS, FAN CTRL
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The over current protection of VDD10 is detected with ILIM pin (No.53) using 180 mOhm of DC resistance (DCR) of inductor L1.
HAR16 should be choosing so that the total resistance of DCR(L1) becomes 180 mOhm.
→ HAR16 + DCR(HAL1) = 180 [mOhm]

Remove

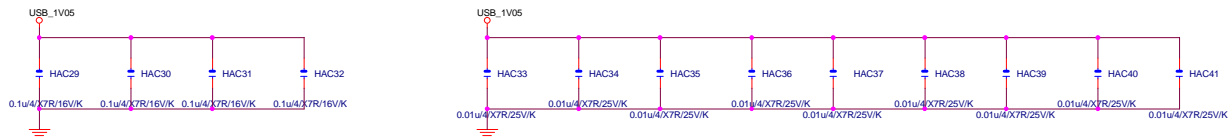
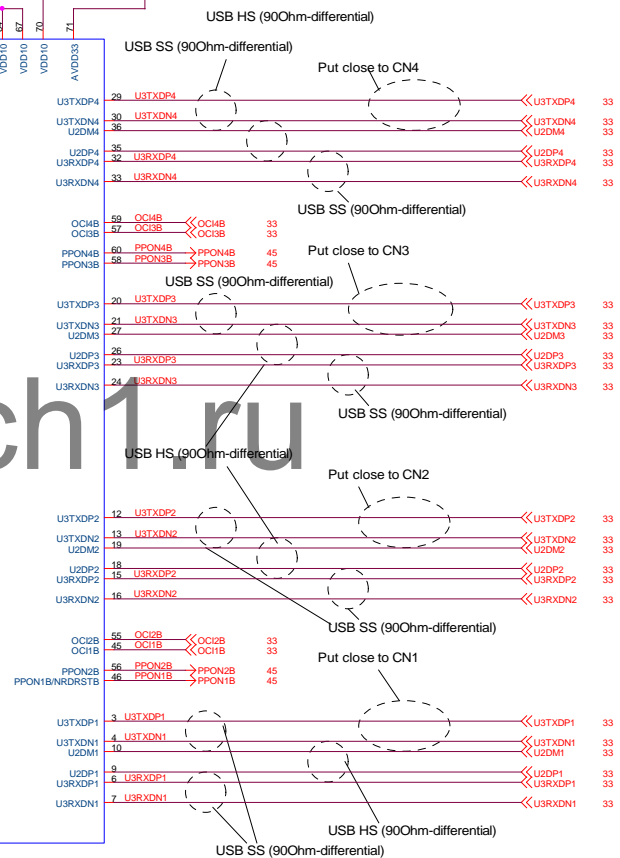
Put close to U1

Put close to U1
Do check with crystal vendor
if the value of C31, C32 and R31 are all appropriate.

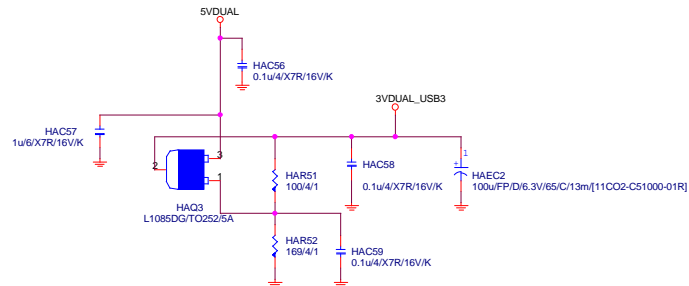
Put close to U1
Short and broad connection to GND
Don't split R32 into multiple resistors.

uPD720210

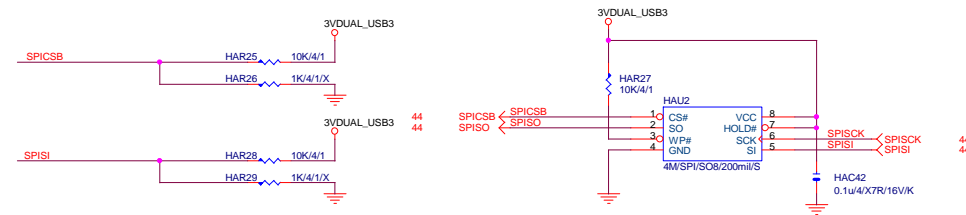
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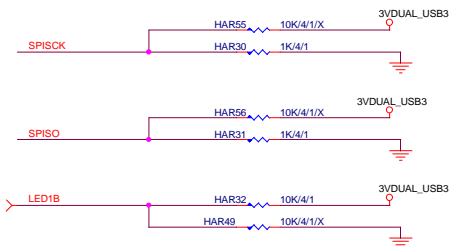
3VDUAL_USB



External SPI ROM ; SPI ROM attached mode

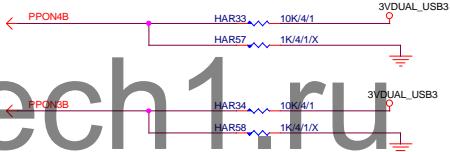


Battery Charging



Number of Ports ; 4Ports mode

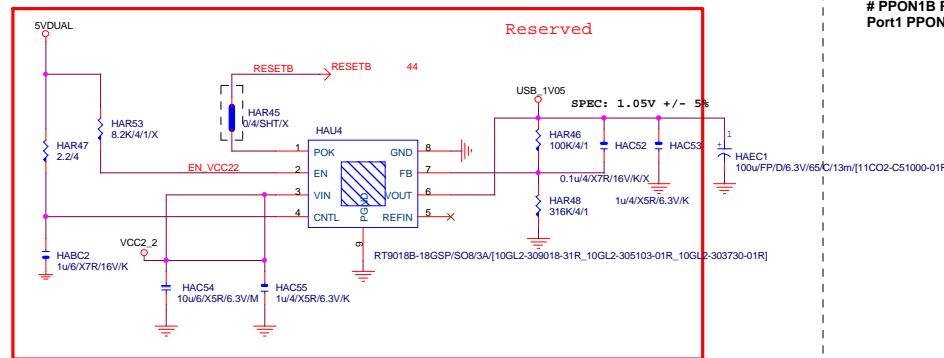
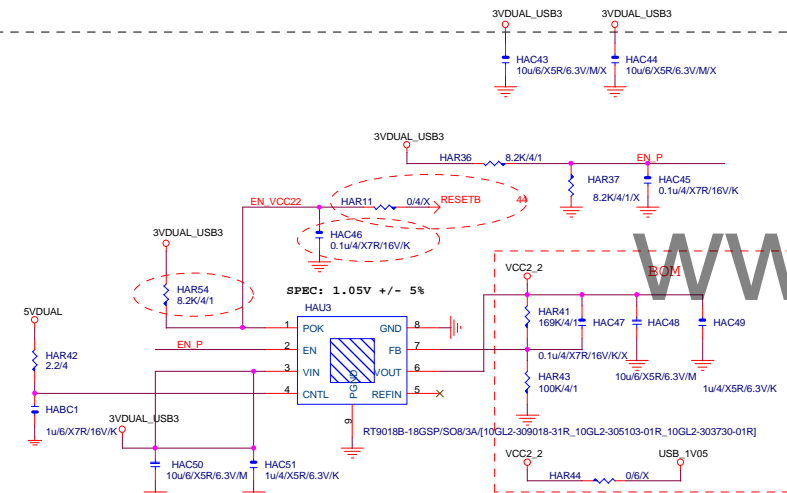
PPON3B / PPON4B : H / H (4 port)
PPON3B / PPON4B : L / L (2 port)



#5 VBUS Power Control ; Individual mode

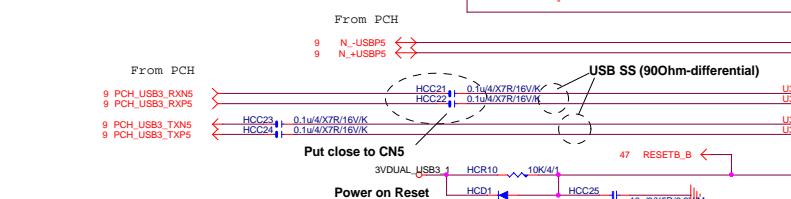
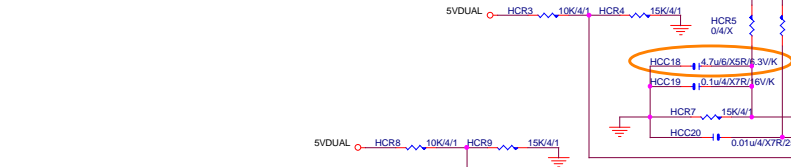
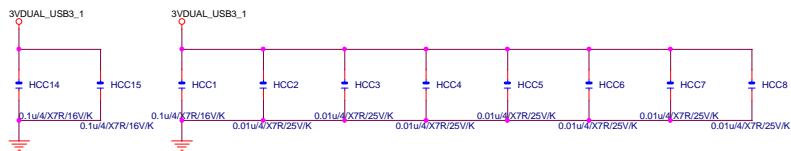


PPON1B Pin Function ; Port1 PPONB mode

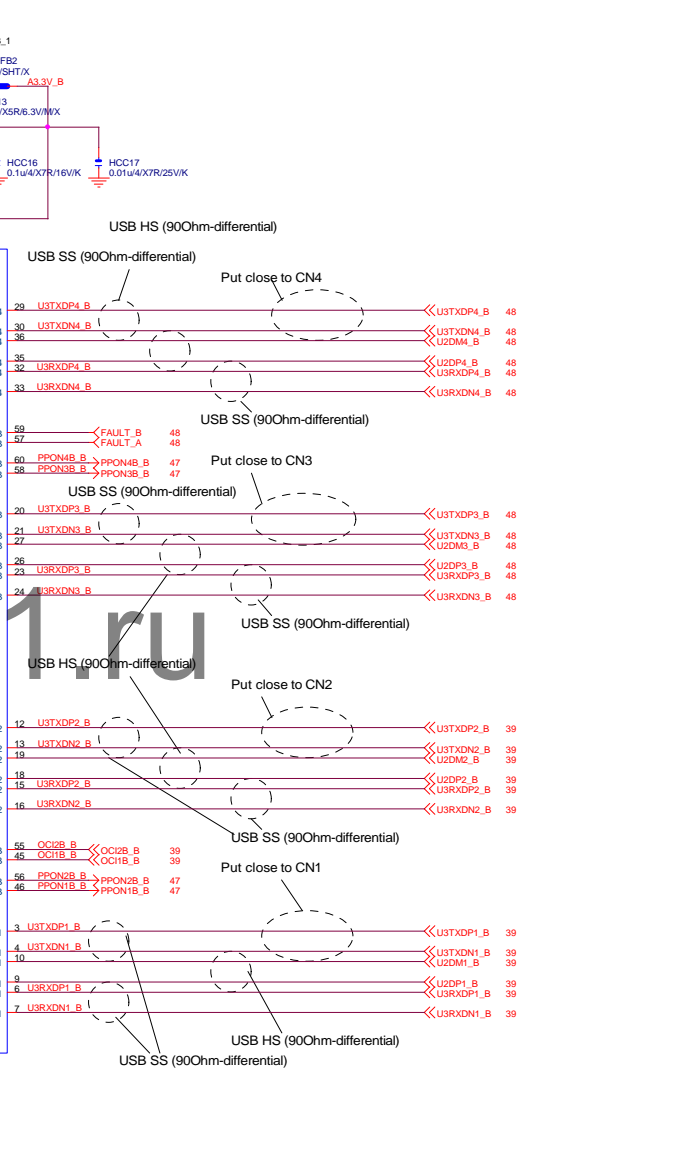
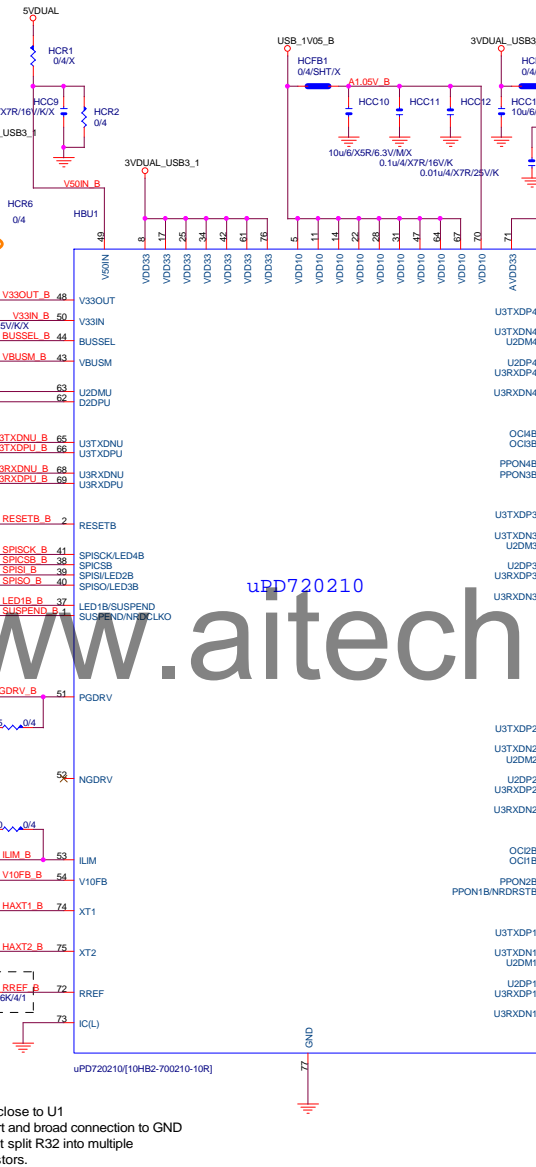
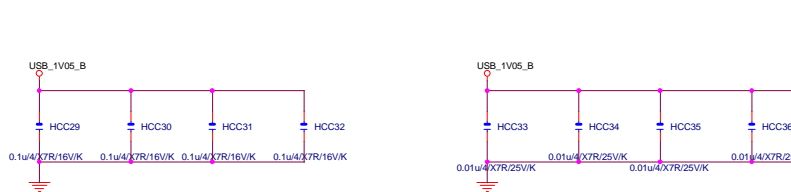
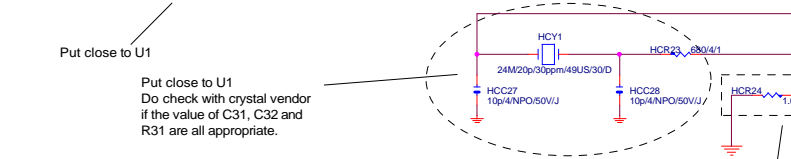
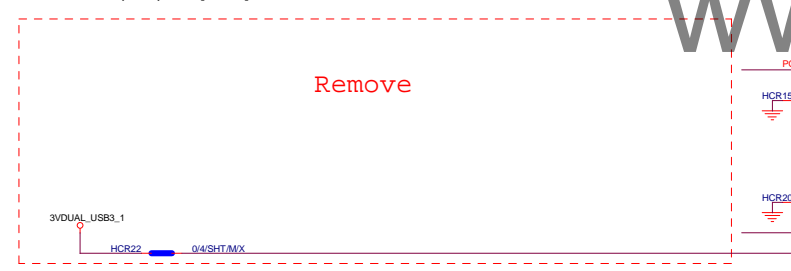


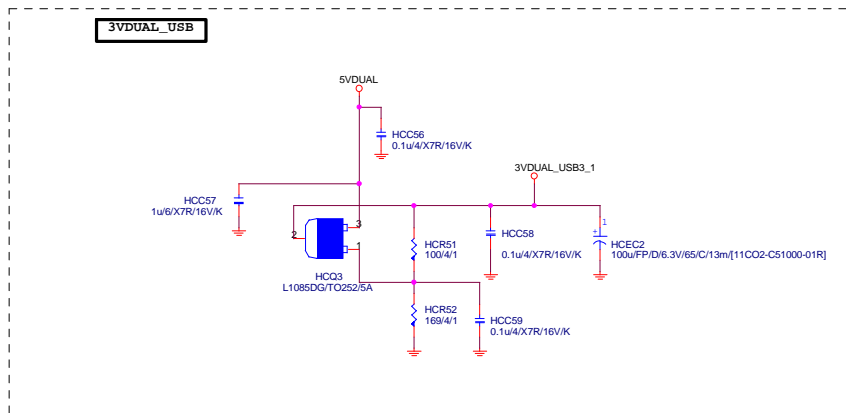
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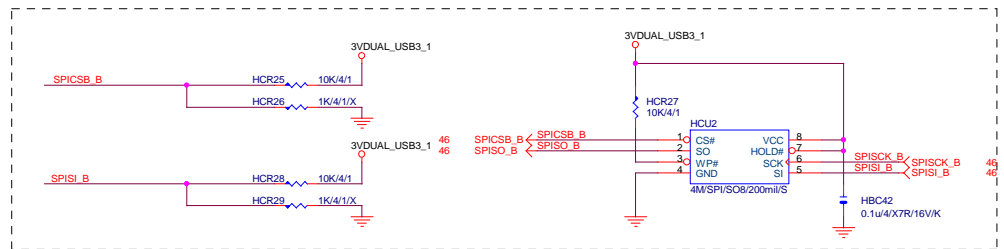


The over current protection of VDD10 is detected with ILIM pin (No.53) using 180 mOhm of DC resistance (DCR) of inductor L1.
HAR16 should be choosing so that the total resistance of DCR(L1) becomes 180 mOhm.
→ HAR16 + DCR(HAL1) = 180 [mOhm]

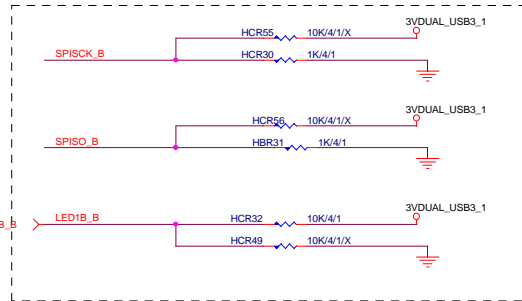




External SPI ROM ; SPI ROM attached mode

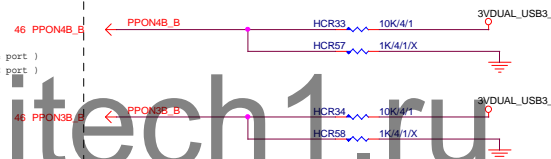


Battery Charging

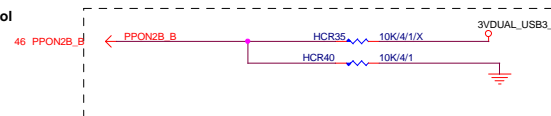


Number of Ports ; 4Ports mode

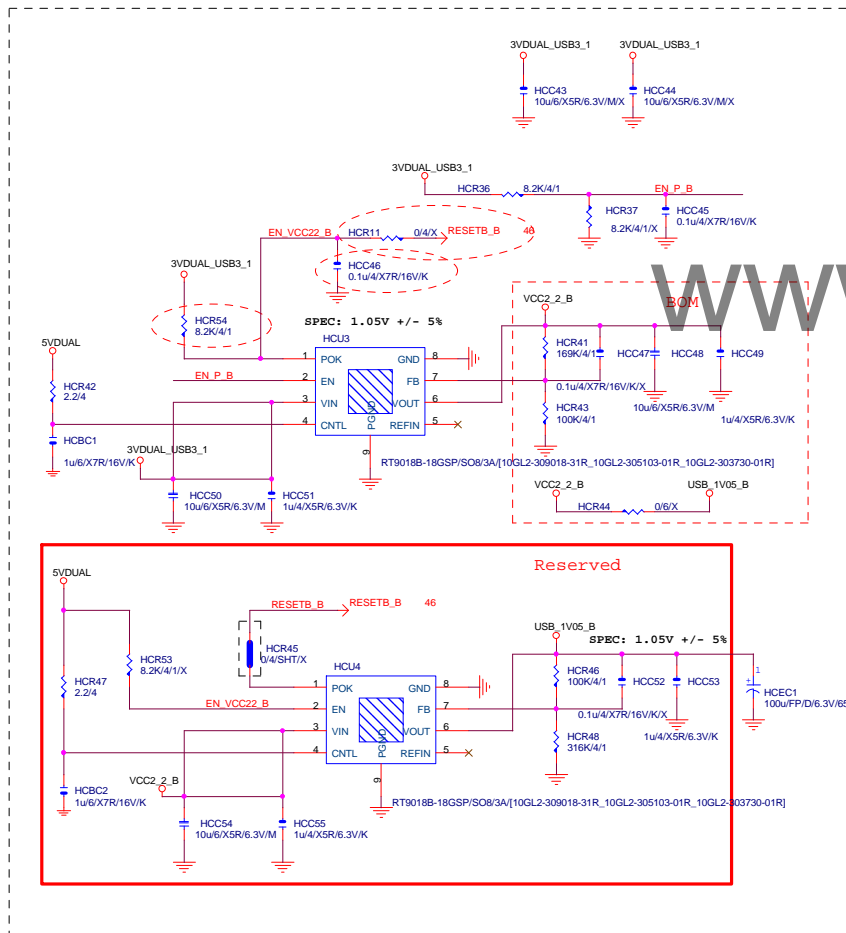
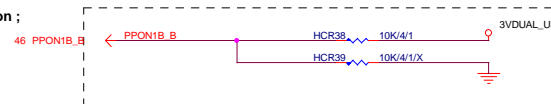
PPON3B / PPON4B : H / H (4 port)
PPON3B / PPON4B : L / L (2 port)

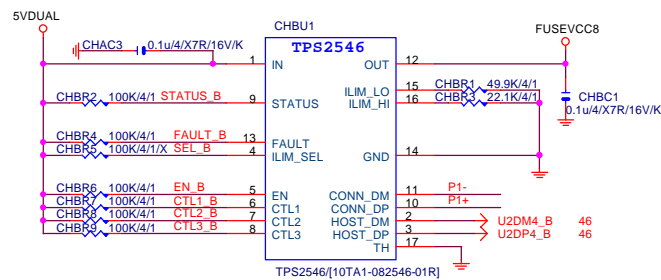
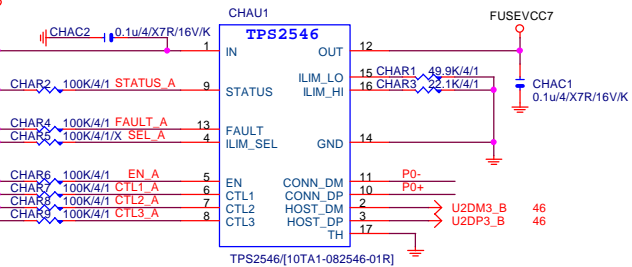
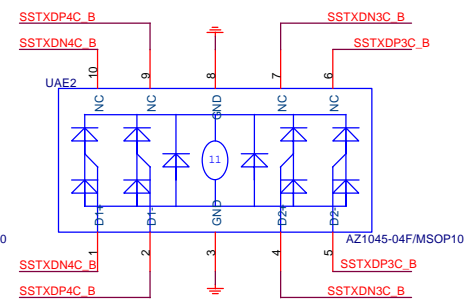
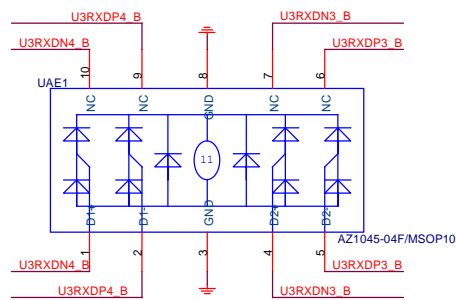
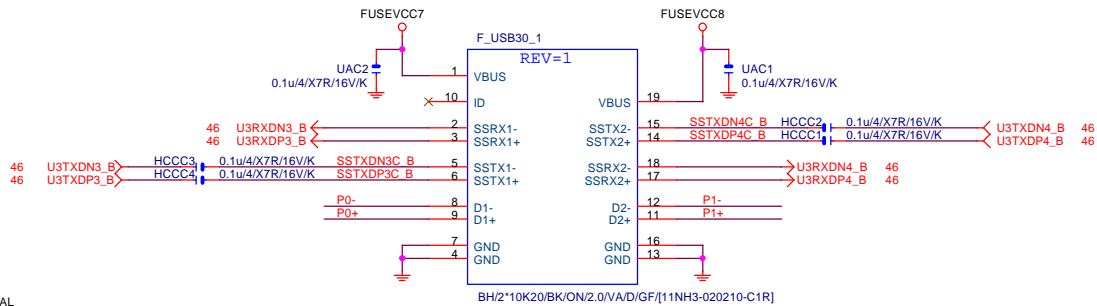


#5 VBUS Power Control ; Individual mode

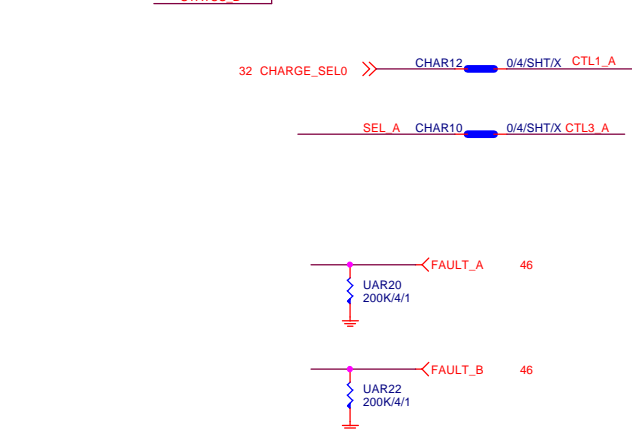
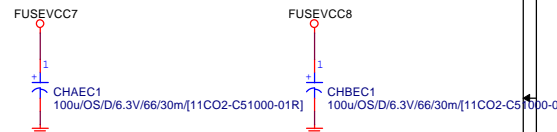
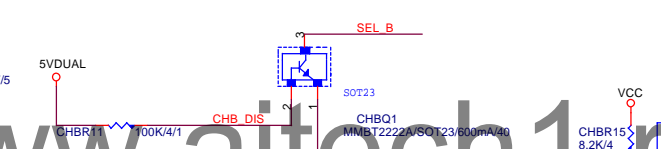
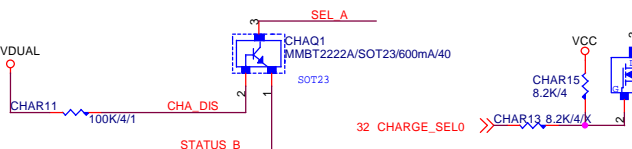
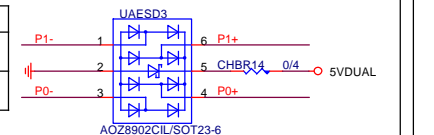


PPON1B Pin Function ; Port1 PPONB mode





	S0	S3/S4/S5
CHARGE_SEL0	1	0
CHARGE_SEL1	1	0



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<Title>		
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